AMIQ EDA Releases Version 19.1 of the Design and Verification Tools Eclipse IDE

Enables More Efficient Creation, Exploration, and Maintenance of HDL Code

SAN JOSE, CALIFORNIA, UNITED STATES, February 25, 2019 /EINPresswire.com/ -- AMIQ EDA, a pioneer in integrated development environments (IDEs) for hardware design and verification and a provider of platform-independent software tools for efficient code development and analysis, today announced that the latest 19.1 release of its Design and Verification Tools (DVT) Eclipse IDE includes important new features for browsing and maintenance of complex hardware description language (HDL) designs. These features include:

- Easier navigation through automatically generated schematic diagrams
- Automatic generation of power supply network diagrams from power intent descriptions
- Verification breadcrumb bar for faster traversal of testbench code
- Scope breadcrumb bar for faster traversal of HDL code hierarchies
- Project database query and visualization capabilities for C/C++/SystemC code

“Intuitive visualization and navigation are at the very heart of using an IDE to develop and maintain design and verification code,” said Cristian Amitroaie, CEO of AMIQ EDA. “The new features in DVT Eclipse IDE have already proven very popular with users and make it even more compelling for anyone using HDLs to choose our solution.”

DVT Eclipse IDE has long had the ability to generate schematic diagrams from HDL code. Connections and relationships among design blocks may be easier to grasp in visual form, especially for complex paths involving many blocks and signals. The new capabilities make it much easier to navigate schematics by expanding, collapsing, and hiding blocks to focus on those of primary interest. The IDE can display only those signals that connect selected blocks. Only a simple series of clicks is required to trace signals with sources and destinations deep within different hierarchies of the design. A demonstration of these capabilities is available at https://youtu.be/6SvN269GTJk.

Power domains are a widely used mechanism to help manage power consumption in system-on-chip (SoC) designs. A single chip may have dozens or even hundreds of domains that run at different power levels and to turn on and off independently. These are specified using one of the two popular power intent formats: IEEE Std. 1801-2015--based on the Unified Power Format (UPF)--and Common Power Format (CPF) 2.0 from the Silicon Integration Initiative (Si2). DVT Eclipse IDE can now generate power supply diagrams from either of these two formats, showing all power domains and the connections between them. The elements in the diagrams are linked to the power intent file source, making it easy to switch between the two views. It is also possible to select a power control signal in the diagram and jump to the location in the design HDL code where it is defined. More on this new feature is shown at https://youtu.be/L8nIA-k0wUA.

The concept of breadcrumbs—hyperlinks stepping through a hierarchy—is familiar to anyone who uses a filesystem or Internet browser. Breadcrumbs are equally applicable for IDEs, providing an easy way to traverse the HDL hierarchies. DVT Eclipse IDE has long had a design breadcrumb bar and has now added a verification breadcrumb bar and a similar capability for traversing scopes. Users can navigate multiple levels of enclosing scopes by simply clicking on the appropriate breadcrumbs. The breadcrumbs are automatically updated as users move

through the source code. DVT Eclipse IDE moves beyond traditional breadcrumbs to show all lower scopes available. These new capabilities are demonstrated at https://youtu.be/37iHQO5XzeQ.

The new release of DVT Eclipse IDE also adds enhanced project database query and visualization support for C/C++/SystemC code, providing similar capabilities to those available for HDL code. New views include C/C++/SystemC types, macros, and files (in order of compilation). Engineers can quickly locate types, classes, macros, etc. by typing a few letters into search bars. This makes it faster and easier to locate elements within C/C++/SystemC models.

In addition to these navigation and visualization highlights, the latest release of DVT Eclipse IDE has a new references engine running behind the scenes. This engine accelerates common tasks such as showing all usages of signals and renaming elements in the design or verification code.

Availability and Pricing

Support for all the new features is available today via DVT Eclipse IDE. Pricing is available upon request. Demonstrations and more information will be available at DVCon US 2019, February 25-27 in San Jose, Calif. AMIQ EDA will exhibit in Booth #405 and will showcase all its products: DVT Eclipse IDE, DVT Debugger, Verissimo SystemVerilog Testbench Linter and Specador Documentation Generator.

About AMIQ EDA

AMIQ EDA provides design and verification engineers with platform-independent software tools that enable them to increase the speed and quality of new code development, simplify debugging and legacy code maintenance, accelerate language and methodology learning, improve testbench reliability, extract automatically accurate documentation, and implement best coding practices. Its solutions, DVT Eclipse IDE, DVT Debugger, Verissimo SystemVerilog Testbench Linter, and Specador Documentation Generator have been adopted worldwide. AMIQ strives to deliver high quality solutions and customer service responsiveness. For more information about AMIQ EDA and its solutions, visit www.amiq.com and www.dvteclipse.com.

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