

# AMIQ EDA Announces Advanced Comparison and Filtering Capabilities for Analysis of Testbench Coding Violations

*New Capabilities in Verissimo SystemVerilog Testbench Linter Accelerate Debug, Reducing Chip Verification Time for Earlier Tapeout*

SAN JOSE, CA, UNITED STATES, February 27, 2020 /EINPresswire.com/ -- [AMIQ EDA](#), a pioneer in integrated development environments (IDEs) for hardware design and verification and a provider of platform-independent software tools for efficient code development and analysis, today announced that its Verissimo SystemVerilog Testbench Linter includes advanced features for comparing reports of rule violations and intelligently filtering the results. This yields much less time spent in examining lint reports and debugging reported violations, speeding verification and reducing project duration.



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*Cristian Amitroaie, CEO of  
AMIQ EDA*

Testbench linting is a highly productive step in the verification process, enforcing coding standards and finding important classes of errors long before any simulation tests are run. However, Verissimo runs often include legacy code and contributions from other verification engineers, sometimes producing thousands of errors and warnings. This makes it hard for an individual user to focus only on the violations in his or her new code without being distracted by messages based on other

parts of the testbench.

The new capabilities of Verissimo address this challenge directly. A user can run Verissimo and generate a baseline report, which may contain many irrelevant violation messages, run again after adding new testbench code or fixing errors, and ignore any violations common to the two

runs. Intelligent filters enable viewing new violations, confirming violation fixes, and assessing the effects of any changes to the coding rules. The common violations can be viewed at any time; they are not suppressed or waived, so they are not forgotten. Some of these violations may be addressed later in the project or by other engineers working on the testbench, but in the meantime they are “noise” and so ignoring them is a productivity boost.

“Legacy testbench code may generate many lint violations, but these can distract from the primary task of checking new code,” said Cristian Amitroaie, CEO of AMIQ EDA. “In fact, project management may decide not to make any changes to legacy code because it is known to work, however ugly it may be. The new compare and linting features of Verissimo allow users to ignore this ‘technical debt’ without the significant manual effort to specify waivers and without the risk of hiding violations that should be considered at some point in the project.”

### Availability and Pricing

The new capabilities are available today in Verissimo SystemVerilog Testbench Linter. Pricing is available upon request. Demonstrations and more information will be available at the Design and Verification Conference (DVCon), March 2-4 in San Jose, California. AMIQ EDA will exhibit in Booth #405 and will showcase all its products: DVT Eclipse IDE, DVT Debugger, and Specador Documentation Generator in addition to Verissimo.

### About AMIQ EDA

AMIQ EDA provides design and verification engineers with platform-independent software tools that enable them to increase the speed and quality of new code development, simplify debugging and legacy code maintenance, accelerate language and methodology learning, improve testbench reliability, extract automatically accurate documentation, and implement best coding practices. Its solutions, DVT Eclipse IDE, DVT Debugger, Verissimo SystemVerilog Testbench Linter, and Specador Documentation Generator have been adopted worldwide. AMIQ strives to deliver high quality solutions and customer service responsiveness. For more information about AMIQ EDA and its solutions, visit [www.amiq.com](http://www.amiq.com) and [www.dvteclipse.com](http://www.dvteclipse.com).

Cristian Amitroaie

AMIQ EDA srl

+40 721 284 254

[email us here](#)

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