Agnisys Delivers Fully Automated, Specification-Based Design and Verification Flow for Registers and Sequences

Three new products generate IP, assemble complete chips, and provide a common front end for SoC automation.

BOSTON, MASSACHUSETTS, UNITED STATES, July 16, 2020 /EINPresswire.com/ -- Agnisys, Inc., the leading EDA provider of the industry's most comprehensive solution for Design and Verification of SoC Hardware/Software Interface (HSI), today announced general availability of three major new products: SLIP-G™, SoC Enterprise™ and IDS NextGen™ (IDS-NG). When combined with existing products, Agnisys now delivers a complete flow from register and sequence specification to assembly, design, verification, and validation of complex system-on-chip (SoC) devices.

Standard Library of IP Generators (SLIP-G) provides an interface for IP customization and configuration and generates the IP register-transfer-level (RTL) designs, testbench models compliant with the Universal Verification Methodology (UVM), and programming sequences. GPIO, I2C, timer, and programmable interrupt controller (PIC) IP is available today, with additional titles in the future based on customer demand.

Assembling the SLIP-G IP and other blocks into an SoC is a huge challenge. SoC Enterprise™ (SoC-E) is a flexible and customizable environment for design assembly of the most complex chips. SoC-E automatically generates RTL aggregators, bridges, and multiplexors as needed by the SoC architecture. SoC-E's Smart Assembler technology automatically integrates and connects these blocks, SLIP-G IP, IP from other sources, and user blocks into a complete SoC.

IDS NextGen™ (IDS-NG) is a specialized integrated development environment (IDE) for large IP blocks and SoCs. It includes a sophisticated GUI for capturing register and sequence specifications. It provides a common front end for SoC-E as well as the IDesignSpec™ (IDS), Automatic Register Verification (ARV™), and ISequenceSpec™ (ISS) products. IDS-NG enables a fully automated design and verification flow for registers and sequences.

From a single specification, used can generate design RTL, complex programming and test sequences, UVM testbench models for simulation, assertions for formal verification, C code for firmware and device driver development, comma-separated-value (CSV) files for Automatic Test Equipment (ATE) post-silicon validation, and user documentation in multiple formats. The Agnisys solution increases productivity, efficiency, and work quality of individual engineers and

project teams, while eliminating system design and verification errors.

“We have long had a vision for a fully automated, specification-based flow for registers and sequences, and our original products made great strides in that direction,” said Anupam Bakshi, Agnisys CEO and Founder. “These three new products complete the flow and deliver on our vision for the benefit of IP and SoC developers worldwide.”

Agnisys will be exhibiting at the virtual Design Automation Conference (DAC) July 20-22, and engineers will be available to discuss the company’s solutions. More information is available at www.dac.com.

About Agnisys
Agnisys, Inc. is a leading supplier of Electronic Design Automation (EDA) software for solving complex design and verification problems for system development. Its products provide a common specification-driven development flow to describe registers and sequences for System-on-Chip (SoC) and intellectual property (IP) enabling faster design, verification, firmware, and validation. Based on patented technology and intuitive user interfaces, its products increase productivity and efficiency while eliminating system design and verification errors. Founded in 2007, Agnisys is headquartered in Boston, Mass. with R&D centers in the United States and India.
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