

## Hirose and eTopus Technology Develop Combined 112Gbps Interconnect Solution for AI Training Applications

Complete bench setup using Hirose mezzanine connectors and eTopus SerDes IP will be demonstrated at DesignCon in San Jose

SAN JOSE, CA, USA, August 17, 2021 /EINPresswire.com/ -- <u>Hirose</u> Electric Co., Ltd., a global leader in connector technology, its design, and manufacturing, and <u>eTopus</u> Technology, a pioneer of ultra-highspeed ADC/DSP-based SerDes for wireline applications including data center, cloud, edge, and 5G base stations, today announced the



development of a 112Gbps interconnect technology built on their products. This combined solution is ideally suited for linking graphics processing units (GPUs) into a fully connected mesh for artificial intelligence (AI) and machine learning (ML) applications. The interconnects use 112Gbps four-level pulse amplitude modulation (PAM4) technology to pack the maximum

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possible bandwidth into each communication channel.

The bench setup demonstrating this solution features the eTopus 112Gbps ePHY<sup>™</sup> SerDes IP evaluation board (EVB) with transmit (TX) and receive (RX) pairs connecting to Hirose's IT-NG or IT14 (IT14 is the second source to Molex Mirror Mezz) mezzanine connector paddle cards via Huber+Suhner connectors and cables, mimicking the full data path of a networking system. Four channels are connected with the worst-case crosstalk configuration using three near end crosstalk (NEXT) aggressors most adjacent to the victim pins in the connector. Pseudo-

random bit stream (PRBS) data traffic is generated at the TX and FIR (finite impulse response)

conditioned signals are then sent through Hirose's interconnect system (with additional insertion loss from the eTopus breakout board). At the EVB RX, analog to digital converters (ADCs) digitize the incoming bit stream, fully adaptive digital signal processing (DSP) equalizes the signal levels, and finally the clock and data recovery (CDR) realizes the data stream. PRBS errors are registered in the error counter and error statistics are used for pre-FEC (forward error correction) and post-FEC bit error rate (BER) analysis.

Hirose is a major supplier to Tier-1 network, system, and cloud providers. Its products include connectors and connectivity solutions for a wide range of applications. The project with eTopus uses a not-yet-formally-released next-generation connector (IT-NG) to leverage state-of-the-art technology. To meet a wide range of different system design requirements, Hirose's IT-NG and IT14 mezzanine connectors offer stack heights ranging from 5mm to 46mm, which allows module/daughter card system design to optimize its mechanical and airflow/thermal designs. In addition to a wide range of stack heights, IT-NG employs three-piece design (two sockets and one interposer), which provides significant manufacturability advantage over two-piece solutions when PCB thermal reflow is needed.

With field polarity swapping cancellation and extended ground shielding into socket, IT-NG significantly suppresses crosstalk (ICN < 1.7mV with all adjacent aggressors enabled) yet still has great signal density (80.3 Diff-Pairs per sq. inch) with a highly configurable total number of signal pins to meet system total bandwidth requirements. The patented reflection minimization design enhances the effective bandwidth way beyond the Nyquist frequency (28GHz) which results in great figure of merit (FOMILD) performance.

eTopus is a provider of serializer/deserializer (SerDes) IP for high-speed communications applications. The eTopus high-speed transceiver architecture substantially enhances system BER performance and CDR robustness while reducing system cost and power consumption for networking, storage, and 5G applications. Their industry-leading technology provides excellent BER for long reach applications, excellent post-FEC with minimal decision feedback equalizer (DFE) error propagation for medium to long reach with crosstalk, and low-latency FEC, suitable for AI types of interconnects.

Combining eTopus' 112Gbps ePHY advanced SerDes architecture with Hirose's mezzanine interconnects, the channel impairments induced correlated errors are minimized without observable bursty symbol errors. This characteristic is critical for the forward error correction (FEC) decoder to correctly recover any erroneous codeword and to reduce the frame loss rate even with a small FEC overhead (or a low coding gain with low latency) scheme to maintain data integrity at 112Gbps operation.

"We were pleased to collaborate with eTopus on this project," said Mr. Tsutomu Matsuo, General Manager of Hirose's High-Speed Interconnect Division. "We were able to demonstrate that our latest connector technology can reliably communicate using advanced SerDes technology. This combination will be valuable to many of our customers." "When developing high-speed IP solutions, it is important to test them in a real-world environment," said Harry Chan, founder & CEO of eTopus. "The Hirose connector allowed us to build a bench setup using our IP in a fully connected mesh. We appreciate their support on this project."

The bench configuration built using the combined interconnect solution will be demonstrated at <u>DesignCon</u> in the McEnery Convention Center in San Jose, Calif., August 16-18. Please visit eTopus in Booth 531 see the demonstration and to learn about its revolutionary ePHY SerDes IP.

## About Hirose Electric Co., Ltd.

Hirose is a global leader in the design and manufacturing of connectors with a wide customer base spanning consumer electronics, industrial equipment, automotive, high-speed networking and storage industries. Hirose specializes in a variety of connector solutions: RF coaxial, boardto-board, board-to-FPC, high speed, power, and automotive to name a few.

Since the inception of Hirose in 1937, the company has developed and introduced thousands of new connectors for numerous applications. The company continues to broaden the scope of its business activities, keeping pace with market advances and satisfying the changing connector needs of companies in Europe, Asia and North America. Hirose's vigorous international strategy rests on three pillars: strong capital investment, a highly skilled labor force, and close contact with the product development divisions of client manufacturers throughout the world.

With the technical knowledge gained from this contact and backed by the company's own human and financial resources, Hirose is dedicated to meeting connector demand world-wide and to contribute meaningfully to progress in connector technology.

For more information please visit: Hirose.com.

About eTopus Technology Inc.

eTopus is an innovator and technology leader in high performance, DSP-based, mixed-signal, ultra-high-speed semiconductor interconnect solutions. Our ultra-high-speed SerDes IP is adopted by global Tier-1 players to be used in networking, storage, 5G, and AI applications. eTopus is a VC-backed startup headquartered in the center of Silicon Valley where our innovations and advanced architectures are developed. Multiple locations are set up globally in USA, Europe and Greater China to provide sales, design and customer support. Our investors include SK Telecom, HK-X, corporate VCs, and cross-border funds. For more information, please visit eTopus.com

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