

eTopus introduces 400G(4x100G) LR IP solution incorporating new FEC & ePHY with combined latency of sub 10ns

SAN JOSE, CALIFORNIA, US, October 19, 2021 /EINPresswire.com/ -- eTopus Technology, a pioneer of ultra-high-speed ADC/DSP-based SerDes for wireline applications is proud to introduce its new [400G](#) Long Range (LR) IP solution incorporating Forward Error Correction (FEC) IP and the eTopus DSP-based production-proven SerDes PHY (ePHY) IP with combined latency of sub 10ns.



The solution has been silicon-proven in 6 and 7nm foundry processes and tested with multiple cable companies and is ready for volume production.

“

The eTopus 400G LR IP solution with their ultra-low latency PHY aligns well with demand from our customers for integrated chiplet solutions ...”

*Mohit Gupta, SVP and GM,
SoC IP at OpenFive*

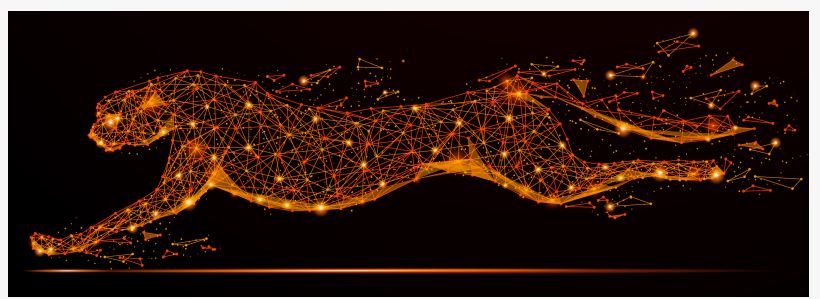
The eTopus high-speed transceiver architecture supports a wide range of data rates for multiple standards, such as Ethernet, OIF CEI-[112G](#), PCI-SIG® PCIe® Gen 1 through 6, and insertion loss from few to above 30dB, while maintaining the sub 10ns latency.

“This 400G LR IP [ultra-low latency](#) solution is the culmination of many years of effort and in response to tier-1 customer demands. Current solutions for FEC and PHY have combined latency in 100ns range and we are pleased to introduce our silicon-proven sub 10ns solution,” said

Harry Chan, founder and CEO of eTopus “Now customers developing switches, NIC cards, DPU, re-timers, and active cables can leverage our 400G LR IP solution to slash latency and directly accelerate system performance.”

“The eTopus 400G LR IP solution with their ultra-low latency PHY aligns well with demand from our customers for integrated chiplet solutions based on OpenFive’s Die-to-Die, Ethernet and

Interlaken Controllers, particularly in High Performance Computing (HPC) and Data Center accelerator applications.” said Mohit Gupta, SVP and GM, SoC IP at OpenFive.



eTopus Ultra-high-speed SerDes IP

Key Background Facts

- BER of $< 1e-17$ is required for data integrity to support customer needs
- For PAM 4 a FEC is mandatory and eTopus solution is a combination of SerDes and FEC IP delivering robust post-FEC BER $< 1e-17$
- Currently just with standard RS(544, 514) FEC, latency is 100ns range which for access time dependent solutions limits performance
- eTopus ePHY SerDes and Ultra Low Latency FEC IP solution easily meets the performance requirement of post-FEC BER $< 1e-17$

About eTopus Technology Inc.

eTopus is the technology leader in high performance, DSP-based, mixed-signal, ultra-high-speed semiconductor interconnect solutions. Our ultra-high-speed SerDes IP is adopted by global Tier-1 players to be used in networking, storage, 5G, and AI applications. eTopus is a VC-backed startup headquartered in Silicon Valley where our innovations and advanced architectures are developed. Our investors include SK Telecom, HK-X, corporate VCs, and cross-border funds. For more information, please visit etopus.com.

About OpenFive

OpenFive, a SiFive business unit, is focused on custom silicon solutions and differentiated IP. With spec-to-silicon design capabilities, customizable SoC platforms, and differentiated IP for Artificial Intelligence, Cloud/Datacenter, High Performance Computing PC, Networking, and Storage applications, OpenFive is uniquely positioned to deliver highly competitive processor agnostic domain-specific SoCs.

The OpenFive IP portfolio includes High-Bandwidth Memory (HBM3/2E) and low power LPDDR5/4x memory subsystems; Die-to-Die (D2D) interface IP subsystems for heterogeneous multi-die connectivity including chiplets; low-latency, high-throughput Interlaken interface IP for chip-to-chip connectivity; 400/800G Ethernet MAC/PCS subsystems, and USB controller IP. OpenFive offers end-to-end expertise in custom SoC architecture, design implementation, software, silicon validation, and manufacturing to deliver high-quality silicon in advanced nodes down to 5nm. For more information, please visit www.openfive.com.

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