

Baum Showcases Power Modeling for AI Chips

Will Showcase PowerBaum at DAC DEC 5-9 at the Moscone Convention Center, San Francisco, CA, USA

SEOUL, KOREA, November 22, 2021 /EINPresswire.com/ -- Baum today launched the latest version of its flagship product PowerBaum, a state-of-the-art power modeling solution for fast and accurate power analysis.

Baum will showcase the latest PowerBaum in Booth #2430 at the Design Automation Conference (DAC), held from Dec 5th to 9th at the Moscone Convention Center, San Francisco, CA, USA.



“

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*Youngsoo Shin, co-CEO of
Baum*

Highlights of PowerBaum’s new capabilities include power modeling for AI chips and power optimization guidelines. Both are key improvements to analyze and fix power “bugs” in realistic software scenarios.

“Power analysis of AI chip is a pain because of high chip complexity as well as variety of usage scenarios that should be checked. PowerBaum is innovative in creating a power model of one processing element, which is instantiated multiple times for array architecture of AI chip.” remarks Youngsoo Shin, co-CEO of Baum. “Power models linked to RTL simulator or emulator enables orders

of magnitude speedup in power analysis, which has been vital for our AI chip customers.”

The Latest Version of PowerBaum

PowerBaum automatically generates power models from design sources and characterizes gate-level behavior to achieve very high accuracy. The power models run in higher abstraction environments, such as RTL/ESL simulation and hardware emulation to achieve orders of magnitude performance improvement compared to competing solutions in the market.

The new release supports power analysis with FSDB files generated in a hardware emulation.

“Baum power models can accurately analyze power consumption considering glitches with emulator-generated FSDB files,” said Joonhwan Yi, Baum’s co-CEO. “Combining implementation-accurate Baum power models with hardware emulation creates an ideal solution for identifying and analyzing power problems under real operating conditions of large systems.” Users have seen over 1,000 times speed-up compared to competing power analysis solutions when PowerBaum is used together with hardware emulation.

A power optimization guideline is provided after generating the dynamic power waveforms. Operational clock gating ratio (OCGR) is the percentage of flops that are gated each cycle. Combining OCGR waveforms with power waveforms and signal waveforms in a single waveform viewer provides an ideal debugging environment to identify and fix power issues.

The new release also provides both speed and accuracy required by AI chip designers to optimize their design. A single power model generated by PowerBaum can be utilized to do power analysis with multiple processing element instances giving designers the freedom to optimize the power consumption of AI chips.

Furiosa AI, a fabless semiconductor company, used Baum’s power analysis suite to lower both peak power and average power consumption of their AI chip, Warboy, and plan to continue applying it in the design of next generation chips. Recently, LX Semicon, one of the largest global display IC companies, adopted PowerBaum in developing their digital driver ICs (DDIs).

PowerBaum 2.9 is shipping today and available globally. Pricing is available upon request.

About Baum

Baum provides electronic design automation (EDA) software and solutions that enable engineering groups in the mobile, artificial intelligence/machine learning, automotive, internet of things (IoT), networking and server markets to fully optimize the energy efficiency of their semiconductor designs. Founded in 2016 by seasoned semiconductor professionals with technical, R&D, and business development expertise, Baum is privately held and funded.

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For more information, contact:

DongChul, Chung
CBO/Baum Co., Ltd.
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