# AMIQ EDA Joins OpenHW Group and Contributes Linting Capabilities for CORE-V Open-Source RISC-V Cores and Testbenches

*Advanced Analysis Is Improving Code Quality, Maintainability, and Performance*

SAN JOSE, CALIFORNIA, UNITED STATES, November 23, 2021 /EINPresswire.com/ -- AMIQ EDA, a pioneer in integrated development environments (IDEs) for hardware design and verification and a provider of platform-independent software tools for efficient code development and analysis, today announced that the company has joined OpenHW Group, a provider of open-source RISC-V processor cores and related IP, tools, and software. AMIQ technology is being used by OpenHW Group in a continuous integration flow to analyze ("lint") CORE-V SystemVerilog testbench code to automatically detect and suggest fixes for a wide range of issues.

> The OpenHW Verification Task Group was impressed that, from the very first runs, the AMIQ EDA solution identified important issues."
>
> *Rick O'Connor, President and CEO of OpenHW Group*

"Simulators and other electronic design automation (EDA) tools detect some types of coding errors, but the OpenHW team was looking for a dedicated linting tool with more capabilities," said Cristian Amitroaie, CEO of AMIQ EDA. "Our solution detects many types of issues, checking more than 700 rules for SystemVerilog and the Universal Verification Methodology (UVM), and offers suggestions for resolving them. Developers and users of OpenHW Group testbenches can be certain that their code is correct and follows industry best practices."

The solution combines AMIQ EDA Design and Verification Tools (DVT) Eclipse Integrated Development Environment (IDE) and Verissimo SystemVerilog Linter, which can run in batch mode or within the IDE. Users can take full advantage of the IDE's interactive environment to

debug reported issues. Features include a smart source code editor, schematics, and diagrams for finite state machines (FSMs), design hierarchies, and class hierarchies.

“The OpenHW Verification Task Group was impressed that, from the very first runs, the AMIQ EDA solution identified important issues,” reported Rick O’Connor, President and CEO of OpenHW Group. “Some of these were violations of our existing SystemVerilog coding guidelines that we previously had no automated way to detect, and some were due to rules we had not considered before. We have confirmed and fixed dozens of these issues, so we have already seen the value of the enhanced linting, and analysis provided by AMIQ EDA.”

As part of the contribution to OpenHW Group, the AMIQ EDA team has established a pre-packaged open-source setup environment that makes it easy for users to continue to run linting on CORE-V testbench components as they integrate them into their system-on-chip (SoC) environments. The environment also allows users to examine and debug the Verissimo results within DVT Eclipse IDE. This setup is now in the OpenHW code repository and available to everyone. The RISC-V architecture has numerous options for user extensions and customizations, so users can also verify the integrity of any SystemVerilog code that they modify or add during the integration process.

AMIQ EDA has also established a continuous integration regression environment that runs lint analysis every six hours to pick up all recent changes to the cores or testbenches in the OpenHW Group repository. Reports are available at www.dvteclipse.com/core5verif-verissimo/1/main/index.html. While individual CORE-V developers are encouraged to take advantage of the pre-packaged environment to verify all code before it is contributed to the repository, proactive regressions ensure that all changes and additions to the code base are verified. AMIQ EDA has been running similar automated regressions for several years on the code in the UVM repository and this has proven highly beneficial. Reports are available at www.dvteclipse.com/uvm-verissimo/1/main/index.html

About OpenHW and CORE-V

The charter of the OpenHW Group is to serve developers of processor cores and hardware and software engineers who design SoCs with greater awareness, understanding and availability of open-source processor implementations for use in high volume production. OpenHW provides an infrastructure for hosting high quality open-source HW developments in line with industry best practices. The cores task group within the organization has the mandate to develop feature and functionality roadmap and the open-source IP for the cores within the OpenHW Group such as the CORE-V Family of open-source RISC-V processors.

The OpenHW Verification Task Group has the mandate to develop best-in-class verification testbench environments for the cores and IP blocks designed by the members of the OpenHW Group. First among these is the CV32E40P, an industrialized version of the PULP RI5CY RV32IMC

embedded class core. The second generation CV32E40P has an optional 32-bit FPU and Xpulp instruction set extensions for Machine Learning and DSP operations. Currently the OpenHW Verification Task Group is focused on the verification of this second generation of the CV32E40P plus two new embedded class cores, the CV32E40X and CV32E40S, and the CVA6, an application class core configurable for 32-bit and 64-bit implementations.  For more information on the OpenHW Group and task group projects visit: www.openhwgroup.org.

About AMIQ EDA

AMIQ EDA provides design and verification engineers with platform-independent software tools that enable them to increase the speed and quality of new code development, simplify debugging and legacy code maintenance, accelerate language and methodology learning, improve testbench reliability, extract automatically accurate documentation, and implement best coding practices. Its solutions, DVT Eclipse IDE, DVT Debugger, Verissimo SystemVerilog Testbench Linter, and Specador Documentation Generator have been adopted worldwide. AMIQ strives to deliver high quality solutions and customer service responsiveness. For more information about AMIQ EDA and its solutions, visit www.amiq.com and www.dvteclipse.com.

Cristian Amitroaie
AMIQ EDA
+40 721 284 254
email us here
Visit us on social media:
Twitter
LinkedIn
Other

---