Agnisys @ DVCON India 2022: Presenting the Latest Release of IP/SoC Design, Co-Verify, Co-Validate, Co-Everything

Agnisys @ DVCON India 2022: Presenting the Latest Release of IP/SoC Design, Co-Verify, Co-Validate, Co-Everything in 45 Minutes! | Agnisys

BANGALORE, KARNATAKA, INDIA, August 29, 2022 /EINPresswire.com/ -- Agnisys, Inc., the leading EDA provider of the industry's most comprehensive solutions for SoC development, to present its latest proposal for a complete solution of IP development at the upcoming DVCon India and a workshop on IP/SoC Design, Co-Verify, Co-Validate, Co-Everything in 45 Minutes!.

There is a growing demand to create an automation technique to overcome this manual work of creating application logic in an intellectual property (IP) design. Apart from the addressable register information, the IDS CompleteIP solution helps to capture the design functionality (the application logic) through simple templates, which helps in the overall "Completeness" of an IP. The scope of this defined logic is not limited to the generation of the synthesizable RTL but also extends to the verification of the generateddesign, including its corresponding RAL and automatic test sequences, using AI for maximum code coverage of the created application logic. Agnisys will be discussing the CompleteIP solution at DVCon India in booth number 14.

System-on-chip (SoC) projects are naturally complex, and difficult to complete successfully in a short span of time and with limited resources. From the specification, architecture, RTL design, and software design to verification and validation, all aspects are challenging. The workshop will focus on the challenges faced by SoC developers, driven by the convergence of applications onto a single device, and will suggest methodology improvements using a revolutionary multi-platform solution, such as IDesignSpec NextGen™ (IDS-NG), for creating IPs, stitching them together into an SoC, building software and test sequences for the entire design, and documenting it. This solution provides:

Ability to reuse the IPs
Customizing the designs
Example: adding functionality such as additional fields and registers to the IP's register map
Configuring the designs
Example: setting values for the parameters
Ability to handle different bus protocols for high performance data transfers
Horizontal and vertical reuse

Verification is not the end: firmware, prototype, and validation are also required

Test sequences and register specifications created at block or IP level can be run at subsystem or system level

Changes in bus protocol

Differences in configuration

Differences in the way transaction are carried out

Support for multiple people collaborating on a project

Teams must be able to keep track of changes

The latest release of IDS NextGen is now available for download and free evaluation.

About IDS-NextGen

IDS NextGen™ is a multi-platform product that helps users to create SoC specifications at an enterprise level. It handles individual IP to sub-system to SoC level and is compatible with Word, Excel, IP-XACT, RALF, CSV, SystemRDL, and other formats. IDS NextGen generates design and verification code for not just registers but sequences in one integrated environment. It reduces the verification time by generating the entire UVM SystemVerilog and SystemC output sequences.

About Agnisys

Agnisys, Inc. is a leading supplier of Electronic Design Automation (EDA) software for solving complex design and verification problems for system development. Its products provide a common specification-driven development flow to describe registers and sequences for System-on-Chip (SoC) and intellectual property (IP) enabling faster design, verification, firmware, and validation. Based on patented technology and intuitive user interfaces, its products increase productivity and efficiency while eliminating system design and verification errors. Founded in 2007, Agnisys is based in Boston, Massachusetts with R&D centres in the United States and India.

www.agnisys.com

Anupam Bakshi
Agnisys, Inc.
+1 978-631-0505
email us here
Visit us on social media:
Twitter
LinkedIn

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