

Silicon Frontline Receives EOS/ESD Symposium Outstanding Paper Award

SAN JOSE, CALIFORNIA, USA, October 11, 2022 /EINPresswire.com/ -- [Silicon Frontline Technology](#) is proud to announce that they are a recipient of 43rd Annual [EOS/ESD](#) Symposium Outstanding Paper Award for a paper titled "[Enablement, Evaluation and Extension of a CDM ESD Verification Tool](#) for IC Level". The paper was co-authored with Infineon Technologies and Technical University of Munich.



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Dermott Lynch, COO of Silicon Frontline Technology

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Silicon Frontline's ESRA (Electrostatic Reliability Analysis) is a full-chip ESD analysis solution. It identifies weak points in ESD protection circuit and supports ESD sign-off for both HBM and CDM standards. ESRA delivers extraction, analysis, and debugging capabilities in one integrated

environment with the capacity to analyze the full-chip, validated to 15B transistors. Highlighted violations permit engineers to perform corrections at any time in the design process.

About Silicon Frontline

Silicon Frontline Technology provides the only electrical layout verification solution that addresses the most critical yet difficult to solve performance and reliability challenges in today's electronic designs. Our products enable engineers to improve efficiency and ensure robustness of their designs.

Over 70 electronic companies rely on Silicon Frontline products and services for their silicon success. Silicon Frontline products are widely adopted by IDMs and foundries, including 12 of the top 25 semiconductor companies and have been used in thousands of designs.

Silicon Frontline was founded in 2007 by former members of Nassda, Epic Design, and Quad Design. Our team brings 300+ years of computational geometry, complex numerical methods, and semiconductor material expertise. We are primarily funded by angel investors and iD

Ventures.

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