SIGen Enhances CMOS Performance by 3DIC Wafer Scale Stacking Using Proprietary NANOCLEAVE(TM) Layer Transfer Process

SiGen Extends Application of Industry Proven NanoTec Suite of Process Technology, Tools and Know-how, including NANOCLEAVE(TM) Layer Transfer Process, to 3DIC

FREMONT, CA, UNITED STATES, March 3, 2023 /EINPresswire.com/ -- Silicon Genesis Corporation (SiGen) has extended the application of its industry proven NanoTec suite of process technology, tools and know-how, including the industry standard NANOCLEAVE(TM) Layer Transfer Process, to Three Dimensional Integrated Circuits (3DIC). By stacking less than 2um thick CMOS device layers into atomically bonded, heterogeneous circuit elements, overall system bandwidth and performance is enhanced for applications including stacked CMOS image sensor, logic, memory and MEMS applications.

With the end of the 50-year cycle of systematic IC performance improvement by Dennard scaling of vertical and lateral device dimensions, improvements in electronic systems performance is now driven by combinations of IC chips and sensors in the vertical dimension. Stacking of wafer-scale IC devices into 3DIC systems greatly shrinks data path lengths between logic and memory functions and greatly increases interconnect density to achieve performance levels well beyond capabilities of present day 2.5 and 3D packaging methods.

SiGen collaborates closely with its customers by using its Customer Specific Substrate (CSS) development approach to work on application specific products. CSS is one of the most effective approaches in SiGen's NanoTec tool kit. Through years of collaborative experience with CSS procedures, SiGen and their customers are able to arrive at optimal layer transfer solutions with much shorter development times.

CSS procedures guide SiGen and its customers in mutually adapting their device designs and layer transfer processes to optimize performance for specific applications. This involves addressing issues such as controlling device surface planarity and roughness to obtain strong wafer-to-wafer bonding as well as dealing with various other issues, such as changes in device bow, warp and stress occurring when thin device layers are transferred to planar handle wafers.

The SiGen NanoTec layer transfer tools and processes are built around two key process requirements: (1) strong atomic layer bonding of semiconductor wafers using SiGen Plasma

Activation Technology and (2) efficient room temperature cleaving of layers using its proprietary Room-Temperature Controlled Cleaving Process (rT-CCP) to initiate cleaving and separating layers of material at room temperature through various techniques. This Layer Transfer Process called NANOCLEAVE(TM) has been known as a SiGen industry standard for fabrication of SOI and SOQ wafers for over twenty years.

The extension of the NANOCLEAVE(TM) Layer Transfer Process to 3DIC has been accompanied by granted patents in the U.S. and worldwide that include solutions for: (1) imbedded cooling channels between device layers, (2) lateral interconnect networks that are more dense and involve less distance between active circuit layers than the standard Redistribution Layers (RDL's) used in present day 2.5D packaging, (3) damage mitigation in sensitive dielectric layers, (5) efficient cleave plane formation under circuit elements with widely variable metal interconnect densities and (6) integration of both wafer and die-scale IC devices into heterogeneous 3DIC systems.

SiGen has been actively developing 3DIC process technology for over seven years including several applications for CMOS Image Sensors (CIS). This promising development has the potential for introducing leading edge CIS products that are one or two generations ahead of current competitive products in the market.

SiGen business activities which focus on enabling large-scale implementation of layer transfer methods for 3DIC include: active support of customer development, licensing of technology for transfer to high-volume manufacturing and selling of process enabling tools.

About SiGen

SiGen is a leading provider of engineered substrate process technology and equipment for the semiconductor, display, and optoelectronics markets. SiGen's technology is used for production of Silicon-on-Insulator (SOI) semiconductor wafers and 3DIC stacks of CMOS device layers for high performance applications. SiGen develops innovative substrates through thin-film and thick-film engineering, enabling new applications and markets for its customers. SiGen's customers and partners include top players from substrate, device and equipment suppliers throughout the world. Founded in 1997, SiGen is headquartered in Fremont, California. For more information, visit www.sigen.com for the complete SiGen NanoTec offerings of layer transfer process, equipment technology and services.

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