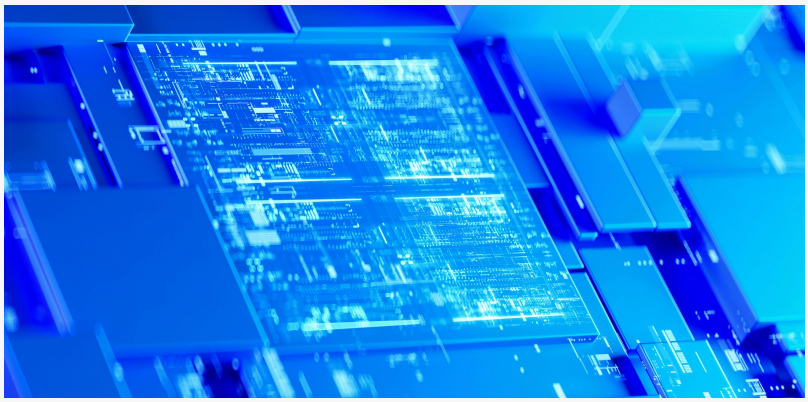
sureCore and Universal Quantum announce tape out of cryogenic IP demonstrator chip

SHEFFIELD, UK, July 7, 2023 /EINPresswire.com/ -- The sureCore-led Innovate UK (IUK) - funded project "Development of CryoCMOS to Enable the Next Generation of Scalable Quantum Computers" has achieved a critical milestone with the tape out of its first cryogenic IP demonstrator chip.



sureCore has exploited its state-of-the-art, ultra-low power memory design skills to create embedded Static Random Access Memory (SRAM), an essential building block for any digital sub-system, that is capable of operating from 77K (-196°C) down to the near absolute zero temperatures needed by Quantum Computers (QCs). In addition, both standard cell and IO cell libraries have been re-characterised for operation at cryogenic temperatures thereby enabling an industry standard RTL to GDSII physical design flow to be readily adopted.

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> *Paul Wells, sureCore CEO*

A key barrier to QC scaling is being able to collocate ever increasingly complex control electronics close to the qubits that must be housed at cryogenic temperatures in a cryostat. In doing so, it is essential that the control chip power consumption is kept as low as possible to ensure that excess heat is kept to a minimum, so it does not cause additional thermal load on the cryostat. Here, sureCore's low power design expertise proved pivotal.

Current QC designs have the control electronics located outside the cryostat as modern semiconductor technology is only qualified to work down to -40°C. As the temperature is reduced close to absolute zero, the operating characteristics of the transistors change markedly. Measuring, understanding and modelling this behavioural change over the past months has culminated in this IP demonstrator chip that will showcase the potential to build cryogenic interface chips that can control and monitor qubits at cryogenic temperatures.

Paul Wells, sureCore's CEO, explained, "Currently, expensive bulky cabling connects room temperature control electronics to the qubits housed in the cryostat. Enabling QC developers to be able to exploit the fabless design paradigm and create their own custom cryogenic control SoCs, which can be housed with the qubits inside the cryostat, is a game-changer that will rapidly enable QC scaling. Immediate benefits include cost, size and, most importantly, latency reduction. The next step will be characterising the demonstrator chip at cryo temperatures to further refine and validate the models to help improve the performance."

The IUK-funded consortium is a complete ecosystem of companies with the expertise and core competencies required to develop cryo-tolerant semiconductor IP. The aim of the project is to develop and prove a suite of foundation IP that can be licenced to designers allowing them to create their own Cryo-CMOS SoC solutions. By doing so their competitive edge in the Quantum Computing space will be dramatically accelerated.

One such consortium member is Universal Quantum (UQ). UQ's modular ion-trap-based, QC hardware architecture will directly benefit from the cryogenic IP developed by the project. Interestingly however, its architecture does not need the sub-4K temperatures used by other QC implementations – especially those based on superconducting qubits. In comparison, its 70K operating environment can be considered quite warm!

There are a large number of QC start-ups around the world and this project will make cryo-IP commercially available for the first time. This will help early adopters fast track their QC solution to market. Wells added, "We are positioning ourselves as the go-to experts in the field of cryogenic IP development and, along with our consortium partners, we are enabling the UK to be seen as a centre of excellence for QC. By working as a focused expert team, the project expects to be able to demonstrate such results in the coming year rather than the many years it would have taken without the support of IUK."

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