

AMIQ EDA Adds Runtime Elaboration of UVM Testbench Code to DVT Eclipse IDE

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/EINPresswire.com/ -- [AMIQ EDA](#), a pioneer in integrated development environments (IDEs) for hardware design and verification and a provider of platform-independent software tools for efficient code development and analysis, today announced that it has added an innovative capability to Design and Verification Tools (DVT) Eclipse IDE. By performing the runtime elaboration of SystemVerilog verification environments compliant with the Universal Verification Methodology (UVM), DVT Eclipse IDE now enables users to view their testbench structures accurately reflecting the configuration at the start of simulation.



Traditionally, IDEs have been able to compile and statically elaborate code, which suffices for many languages as well as chip designs written in SystemVerilog. However, static elaboration is insufficient to reflect the dynamic configuration of UVM testbenches. Runtime elaboration provides many advantages for verification engineers:

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*Cristian Amitroaie, CEO of
AMIQ EDA*

- Determining the value of “for” loop indices at the start of simulation, which affects the number of instances in the testbench
- Determining the triggering of “if-then-else” statements at the start of simulation, which affects the testbench

hierarchy

- Taking into account factory overrides, which customize the characteristics of verification components without editing the source code

- Showing the connections of UVM components to the exact interface instances in the chip design
- Showing UVM configuration database getters and setters sorted by execution order and helping to find the setter of a specific getter
- Showing register maps reflecting address offsets

“Users have been asking us for these capabilities for quite some time,” said Cristian Amitroaie, CEO of AMIQ EDA. “Frankly, this was a big project that affected and enhanced virtually every testbench-related feature that we provide. By working with early adopters, we now have a robust solution that will benefit verification engineers throughout our user community.”

The runtime elaboration is performed by a new execution engine within DVT Eclipse IDE, so users do not have to invoke a simulator to determine the state of the testbench structures at the start of simulation. Users can also add breakpoints, step through the source code, and inspect variable values and call stacks. This allows them to debug the UVM elaboration, which can be quite complex given the power and flexibility of the methodology.

AMIQ EDA will be exhibiting in Booth 1326 at the Design Automation Conference (DAC) in San Francisco’s Moscone Center July 10-12 from 10:00 am to 6:00 pm. Representatives will be available to discuss and demonstrate this new capability as well as all aspects of the AMIQ EDA solutions. For more information on the conference, visit <https://dac.com>.

Availability

Runtime elaboration is available in the latest release of DVT Eclipse IDE at no additional charge for current users. Similar support in DVT IDE for Visual Studio (VS) Code is under development and will be available in the near future.

About AMIQ EDA

AMIQ EDA provides design and verification engineers with platform-independent software tools that enable them to increase the speed and quality of new code development, simplify debugging and legacy code maintenance, accelerate language and methodology learning, improve testbench reliability, extract automatically accurate documentation, and implement best coding practices. Its solutions, DVT Eclipse IDE, DVT IDE for VS Code, DVT Debugger, Verissimo SystemVerilog Linter, and Specador Documentation Generator have been adopted worldwide. AMIQ strives to deliver high quality solutions and customer service responsiveness. For more information about AMIQ EDA and its solutions, visit www.dvteclipse.com.

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