

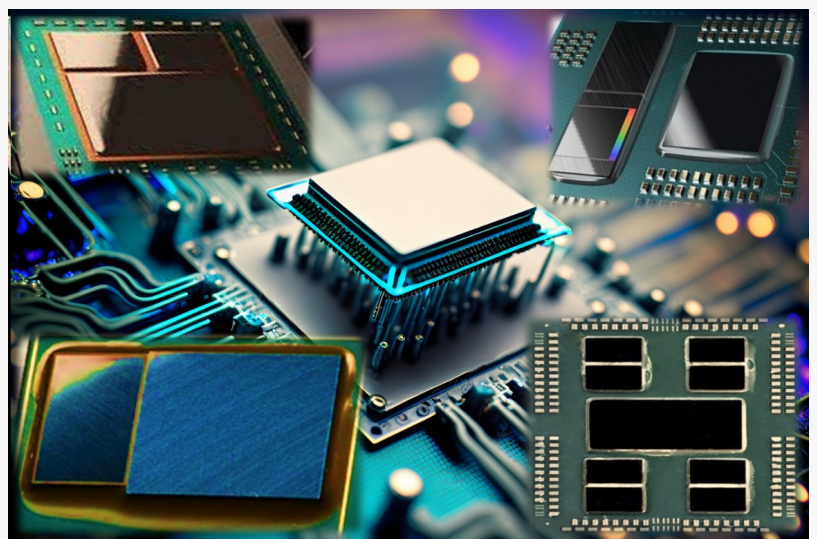
AIT to Introduce Capillary Underfill to Provide Stress Relief with CTE of <math><16 \text{ ppm}/^\circ\text{C}</math> for Stud Bumped Chip with 35 μm Gap

Stress relief underfill for large area chip with copper pillar and gold bumps down to less than 35 μm required different underfilling technology and solution

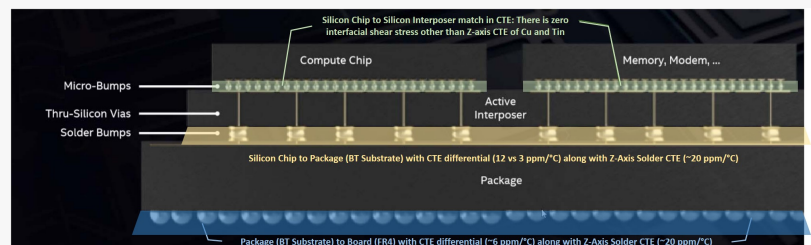
PRINCETON JUNCTION, NJ, UNITED STATES, July 11, 2023

/EINPresswire.com/ -- With more semiconductor design and packaging utilizing fan-in and fan-out wafer level packaging (FO-WLP), underfill that can manage large area chip with copper pillar and gold bumps down to less than 35 μm and advancing toward 25 μm required different underfilling technology and solution.

[AI Technology, Inc.](#) (AIT) have been utilizing its proprietary modified cyanate ester technology to provide both extra-high glass transition (T_g) and low viscosity for fast chip underfill successfully in the last few years. UF-MC7883-FP is a new generation of [capillary underfill](#) solution that have been proven to provide stress relief for chips with less than 35 μm gap. With close to 80% fill with engineered micron sized silica, coefficient of thermal expansion (CTE) has been controlled to less 16 $\text{ppm}/^\circ\text{C}$. The demonstrable [low CTE and high \$T_g\$](#) enable UF-MC7883-FP to provide slight compressive stress and low shear stress for WLP and package-on-package (PoP) and chiplets devices.



Wafer level and chiplets packaging required capillary underfill having much lower CTE and capillary gap-filling than those used in BGA board level packaging. UF-MC7883-FP introduced by AIT has been proven to meet the reliability performance of low CTE and



Chip-on-chip with copper pillar interconnections or gold-stud bumps is best with underfill CTE less than copper at 18 $\text{ppm}/^\circ\text{C}$. Chip-on-package such as BT or equivalent having CTE of 12 $\text{ppm}/^\circ\text{C}$ is best filled with underfill with CTE as close to 12 $\text{ppm}/^\circ\text{C}$ as p

With AIT proprietary stress absorbing modified cyanate ester technology along with its controlled low CTE, even at high Tg of close to 220°C, the shear stress is controlled to minimal level to allow passing of the extreme thermal cycling requirements from -65°C to 150°C for the larger dies of 20mmx20mm. The inherent higher temperature stability of the cyanate ester molecular backbone, its has found some extreme applications at temperature beyond 175°C as well.

For more information on this new generation of low profile underfill for helping to achieve your 3-D chips and chiplets design and reliability, please visit us at booth 1546 of SEMICON WEST 2023.

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AIT Stress Relief Liquid Capillary Underfill				
Liquid Capillary Underfill Properties	UF-MC7883-FP	UF-MC7889-FP	UF-MC7883-NP	UF-MC7883
Coefficient of Thermal Expansion (CTE, ppm/°C, 25°C to 150°C)	16-18	18-20	20-22	22-26
Filler Size Max Cut (µm)	5	5	<0.5	<20
Moisture Absorption and Retention (% 85%RH/85°C/168hr)	<0.5	<0.5	<0.5	<0.5
HAST Reliability (85%RH/ 130°C)	336Hr, Pass	336Hr, Pass	336Hr, Pass	336Hr, Pass
Electrical Resistivity (Ω-cm)	>10 ¹⁴	>10 ¹⁴	>10 ¹⁴	>10 ¹⁴
Dielectric Strength @ 25 Micron Thickness (Volts/mil)	>1000	>1000	>1000	>1000
Dielectric Constant (D _r >1 MHz)	3.2	3.6	3.2	3.2
Dielectric Loss Factor (D _f >1 MHz)	<0.01	<0.01	<0.01	<0.01
Device Push-off Strength (psi)	>3000	>3500	>4000	>4500
Hardness (Type D)	90 (D)	86 (D)	90 (D)	86 (D)
Cured Density (gm/cc)	2.5	2.4	2.2	2.2
Thermal Conductivity (W/m-°K)	>1.5 W/m-°K	>8.0 W/m-°K	>1.0 W/m-°K	>1.0 W/m-°K
Modulus of Elasticity (GPa)	8	8	8	7
Maximum Continuous Operation Temp/Glass Transition Temp(°C)	>180/220	>180/220	>180/220	>180/220
Decomposition Temperature @5% weight loss (°C)	>450	>450	>450	>450
Recommended Capillary Underfilling Gap (µm)	>35	>35	>20	>150

AIT liquid capillary underfill encompasses solutions for wafer level and chiplets packaging required capillary underfill having much lower CTE and capillary gap-filling than those used in BGA board level packaging. UF-MC7883-FP is a new generation that pr

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