YorChip launches UniPHY™ - the first dual-use PHY for Chiplets

YorChip, Inc. launches its UniPHY™ dual-use PHY which enables support of Substrates and Chip Scale Packaging for use on low cost printed circuit boards.

SAN RAMON, CALIFORNIA, USA, July 25, 2023 /EINPresswire.com/ -- YorChip, Inc. today launched its patent pending UniPHY™ dual-use PHY which enables developers to support both traditional Chiplet substrate-based packaging as well as Chip Scale Packaging for use on traditional printed circuit boards.

Chiplets represent multi-billion-dollar market potential – according to Transparency Market Research (https://www.transparencymarketresearch.com/chiplets-market.html), the Chiplet market is expected to reach more than US$47 Billion by 2031, representing one of the fastest growing segments of the semiconductor industry at more than 40% CAGR from 2021 to 2031. This growth is expected to be enabled by the considerable cost reduction and improved yields chiplets will enable as compared to traditional system-on-chip (SoC) designs.

Chiplets can offer the ultimate system design flexibility – however Chiplets have been limited to High Performance Computing environments using the most advanced technology nodes with per unit device costs in the tens to hundreds of dollars. With UniPHY™, YorChip is democratizing Chiplets, enabling lower cost solutions with the ultimate flexibility of packaged Chiplets. Today, the lead-time and NRE cost to develop the custom substrate, chiplet package and system level test can easily exceed $500,000 and take more than six months. YorChip's solution accelerates the design cycle to a few weeks and reduces costs by more than 80%.

"We are excited to announce the first dual-use Chiplet PHY," says Kash Johal, CEO of YorChip. "Our mission is enabling Chiplets for mass markets, and this patent-pending technology will be key to unlocking pervasive use of Chiplets in mass markets for all customers, small, medium and large."

"The key invention here is simultaneously supporting the spectrum of ESD standards for Chiplets in die form (50V) and traditional packages (250V)," explained Ahmad Tavakoli, VP Analog of YorChip" while maintaining ultra-low power of chiplets over traditional I/O such as LVDS/GPIO. Packaged Chiplets are suitable for customers seeking fast time to market, more robust markets and low cost solutions."

Availability
Early customers are already designing with UniPHY™ and finished Chiplets will sample in Q3 2024 with volume production in early 2025.

About YorChip
Silicon Valley start-up focused on Chiplets for Mass Markets. We are leveraging proven partner IP and our novel die-to-die technology to deliver off-the-shelf, low cost, secure chiplets at scale. We are developing a complete ecosystem of off the shelf Chiplets. www.yorchip.com

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