StreamDSP Announces Forward Error Correction (FEC) Capability for High-Speed sFPDP Links

COLUMBUS, OH, USA, August 16, 2023 /EINPresswire.com/ -- Today, StreamDSP LLC, an Intellectual Property (IP) provider specializing in high-speed sFPDP IP cores for FPGAs and ASICs, announced the immediate availability of its StreamFEC Forward Error Correction (FEC) IP core. The StreamFEC IP is designed to integrate seamlessly into the StreamDSP VITA 17.1 sFPDP and VITA 17.3 sFPDP Gen3 IP products. The StreamFEC IP uses a Reed-Solomon (255,239) engine to provide a net coding gain of 5.8dB at 10-13 BER with less than 7% overhead. The StreamFEC IP provides real-time link health and error correction status to the user.

“Our customers are constantly pushing the envelope in terms of data throughput and transmission reliability,” said StreamDSP CTO, Brian Kahlig. “As serial link speeds continue to increase, forward error correction becomes more important. We have designed the StreamFEC IP core to provide FEC protected high-speed serial links across all FPGA vendors and device families as well as ASIC designs. Our ubiquitous device support allows customers to communicate between multiple devices, boards, or systems using FEC protected high-speed serial links with a common protocol and user interface.”

The StreamDSP sFPDP cores provide high-speed, low-latency data links designed for use in a variety of applications including data acquisition, machine vision, and high-performance computing. The new FEC capability is available for all FPGA vendors and device families with data rates up to 32 Gbps per lane. FEC is a data link layer technique that is used to detect and correct errors in digital data. It is an important tool for ensuring data integrity in applications where data loss is not an option.

To facilitate rapid customer integration and ensure success, StreamDSP provides hardware tested example designs, simulation models, and testbench environments for all FPGA families from Altera/Intel, Xilinx/AMD, and Microsemi. Every IP sale includes 12 months of support and maintenance. StreamDSP’s customer base includes defense, industrial, and educational institutions. StreamDSP also provides customized engineering design and integration services.

About StreamDSP LLC: StreamDSP LLC is an Intellectual Property and Engineering Services company based in Columbus, OH. Founded in 2007, StreamDSP has designed Interlaken and Serial Front Panel Data Port (sFPDP) IP cores for FPGAs and ASICs. StreamDSP provides ongoing support and maintenance for their large customer base and also offers custom engineering design services.

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