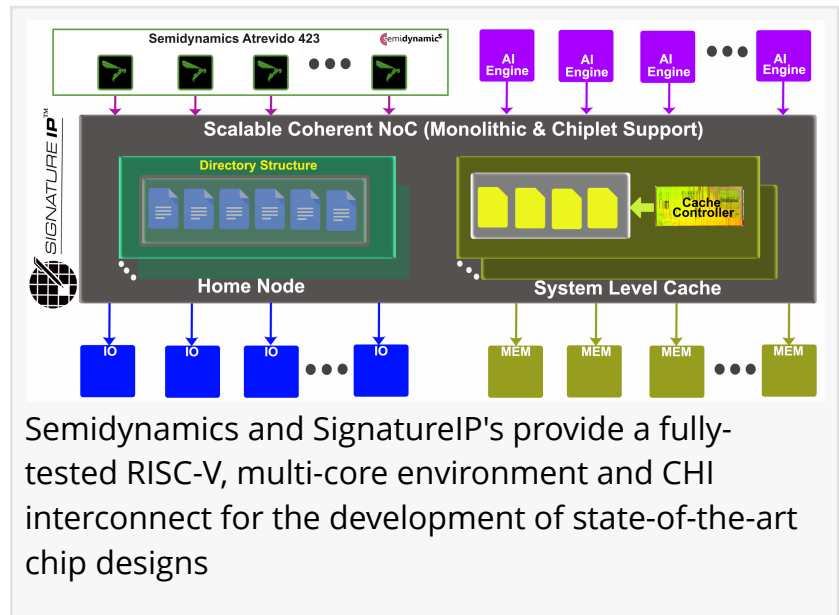


# Semidynamics and SignatureIP create a fully tested RISC-V multi-core environment and CHI interconnect

*Advanced multi-core RISC-V chips can now easily be created for applications such as AI and ML*

BARCELONA, SPAIN, October 3, 2023 /EINPresswire.com/ -- There is an ever-increasing demand for more powerful chip designs for advanced applications, such as AI and ML, that require many cores on one chip. To facilitate this, [Semidynamics](#) and [SignatureIP](#) have partnered to integrate their respective IPs to provide a fully-tested RISC-V, multi-core environment and CHI interconnect for the development of state-of-the-art chip designs.



Semidynamics' CEO and founder, Roger Espasa, said, "Working closely together with other members of the RISC-V community is one of the driving forces of RISC-V's rapidly growing success. There is a natural synergy between the two companies that has resulted in a solution that enables cutting edge, multi-cores chips to be created. SignatureIP's C-NoC CHI interconnect solution makes it very straightforward to lay out the Network on Chip (NoC) for multiple cores on a chip using our mature, proven technologies which minimizes risks and accelerates time to market."

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Semidynamics revolutionized the 64-bit RISC-V processor with cores that are fully customizable using its 'Open Core Surgery' approach."

*Kishore Mishra, SignatureIP's CTO*

SignatureIP's Coherent NoC is architected for performance and scalability across chiplets. It supports a transport layer

for chiplet communication. The C-NoC IP is a directory-based architecture with distributed home-node support and optional system level caches for high performance. SignatureIP's state-of-the-

art inoculator.ai tool supports automation to generate a physically-aware NoC for a system. Combined with the automation tool and a simple licensing model, the process of evaluation, licensing, and implementation becomes an easy task for SignatureIP's customers.

Kishore Mishra, SignatureIP's CTO, added, "Semidynamics revolutionized the 64-bit RISC-V processor with cores that are fully customizable using its 'Open Core Surgery' approach. This goes deep into the core and is not the tweakable approach typically found in IPs. Combining our technologies now enables multi-core chip designs to be created on this fully coherent RISC-V/CHI platform and then prototyping on an FPGA to demonstrate the integrated performance. We have fully tested them together to ensure compatibility and minimization of verification time."

SignatureIP [www.signatureip.ai](http://www.signatureip.ai)

Founded in 2021, Signature IP develops advanced Network-on-Chip (NoC) solutions that form the basis for a comprehensive platform for SoC design. The team boasts over 120 person-years of engineering leadership, specializes in interconnect, networking, datacenter, storage and connectivity IP, from specification to production. The mission at Signature IP is to speed SoC design by easily enabling modifications the NoC topology, various configuration settings, and instant result simulations. Once customers are ready to prototype or implement the NoC, our pushbutton RTL generation integrates directly with customers' EDA and FPGA environments. SaaS tool architecture simplifies tool access and minimizes the burden on their IT department. Enquiries to [contact@signatureip.ai](mailto:contact@signatureip.ai)

Semidynamics [www.semidynamics.com](http://www.semidynamics.com)

Founded in 2016 and based in Barcelona, Spain, Semidynamics™ is the only provider of fully customisable RISC-V processor IP and specialises in high bandwidth, high performance cores with vector units targeted at machine learning and AI applications. The company is privately owned and is a strategic member of the RISC-V Alliance.

Enquiries to [info@semidynamics.com](mailto:info@semidynamics.com)

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