SignatureIP Networks-on-Chips (NoCs) to Accelerate RISC-V Designs

MILPITAS, CALIFORNIA, UNITED STATES, August 14, 2024 /EINPresswire.com/ -- SignatureIP, the pioneer of next generation interconnect and interface solutions, announces that its Networks-on-Chips (NoCs) provide the necessary infrastructure to efficiently connect and manage RISC-V CPUs in complex chip designs. The SignatureIP NoCs offer scalability, flexibility, optimized performance, power efficiency, and interoperability—all key requirements for modern semiconductor designs that bring together the RISC-V architecture and a strong NoC companion.

Purna Mohanty, CEO, SignatureIP, said, “SignatureIP was founded with the goal of making every customer’s SoC optimized to exploit the full speed and efficiency of the most modern interconnect available. When we set out on initial product development in 2021, it was clear that the processor landscape was undergoing a fundamental shift, from industry-wide dependence on one main architecture to encompassing an open-source revolution. Therefore, processor agnosticism is fundamental part of SignatureIP’s development philosophy.”

SignatureIP’s NoC solutions are designed to align with RISC-V CPU requirements:

• Scalability: To support the varying configurations and sizes of RISC-V CPUs, SignatureIP’s NoCs can efficiently scale to connect these different cores together, managing communication between them and other system components without bottlenecks.

• Flexibility: With the custom nature of many RISC-V CPUs, SignatureIP’s NoCs are flexible, allowing designers to customize the network architecture to meet the specific requirements of the RISC-V cores they are integrating.

• Performance Optimization: SignatureIP’s NoC architecture supports optimized routing algorithms and protocols that can handle the high-speed data transfers and low-latency communication needed by RISC-V cores, while keeping a tight power and size envelope.

• Power Efficiency: SignatureIP’s NoCs are designed to minimize power consumption while maintaining the highest throughput, aligning well with the highly energy-efficient characteristics

of RISC-V cores.

• Interoperability: As the RISC-V ecosystem continues to grow, interoperability is crucial. SignatureIP's NoCs support industry-standard interfaces and protocols, ensuring seamless integration with other IP blocks and peripherals typically found in RISC-V based designs.

RISC-V Industry Support for SignatureIP NoCs

Roger Espasa, CEO and Founder, of Semidynamics, a European supplier of RISC-V IP cores specializing in high-bandwidth, high-performance cores with vector units targeted at machine learning and artificial intelligence applications, says, "The close collaboration between members of the RISC-V community is one of the driving forces of the architecture's rapidly growing adoption. There is a natural synergy between the offerings of Semidynamics and SignatureIP – which have been fully tested together to ensure compatibility and minimal verification time. By combining our technologies, customers can create multi-core chip designs on a fully coherent RISC-V/CHI platform and then prototype them on an FPGA to demonstrate the integrated performance."

According to Mike Eftimakis, VP Strategy and Ecosystem at Codasip, a leader in RISC-V custom compute solutions, "At Codasip, we are focused on enabling designers to customize their solutions to significantly improve their PPA. This is uniquely enabled by the flexible RISC-V ISA. By collaborating with partners such as SignatureIP, we can leverage diverse expertise to enhance RISC-V's modular and extensible architecture and accelerate the deployment of RISC-V in high-performance computing as well as embedded systems. By working together, we ensure the continued evolution and widespread adoption of RISC-V as a pivotal force in the future of computing."

Samuel Chiang, Deputy Director of Marketing at Andes Technology, a leading supplier of high-performance/low-power RISC-V processor IP, says, "SignatureIP's NoC solutions, with a focus on interoperability and configurability, are entering the market at the right time. Designers must be able to integrate high-performance, low-power CPU IPs like those from Andes, without added interconnect complexity. SignatureIP's easily accessible cloud-based iNoCulator tool can help customers accelerate innovation and continue to proliferate the RISC-V architecture."

According to John Ronco, SVP Product at RISC-V compute pioneer SiFive, "As SoC complexity continues to increase, NoC requirements are likewise increasing. Customers need best-in-class processor IP as well as efficient, flexible and scalable NoCs that will work seamlessly together. SignatureIP's iNoCulator tool is a welcome addition to the NoC field."

Mukesh Sukla, Head R&D and Customer Success at Marquee Semiconductor, a global leader in chip design solutions, said, "As a provider of design services for complex mixed-signal SoCs, our projects include high-speed connectivity protocols, chiplet-based designs and AI/ML accelerators. For those designs requiring a NoC, we partner with SignatureIP because of the company's

flexibility, support and highly configurable solutions – both coherent and non-coherent NoCs, depending on the project."

About SignatureIP

SignatureIP is building the industry's first web-based Network-on-Chip (NoC) design and development tools, and a portfolio of high-performance NoC Interconnect IP and High-Speed Interface (PCIe, CXL) IPs for developers of AI/ML, HPC and other systems-on-chip (SoCs). SignatureIP offers the industry's first web-based, fully customer-configurable "DIY" NoC development tool for both monolithic and chiplet-based SoCs that lowers the entry barrier for SoC architects and developers. The company also offers the lowest-power, highest-performance PCIe Gen6 and CXL 3.0 IPs on the market based on a ground-up fresh design without the legacy overhead of existing competitors. SignatureIP was founded in 2021 and is based in Milpitas, California. See: https://www.signatureip.ai/.

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