

Agnisys to Showcase AI Chip and FPGA Centric Products at DVCon U.S. 2025 with Exhibit and Accellera Workshops

Agnisys to showcase AI chip and FPGA solutions at DVCon U.S. 2025 with an exhibit and Accellera workshops on IP-XACT & CDC/RDC standards.

BOSTON, MASSACHUSETTS, USA, INDIA, February 24, 2025
/EINPresswire.com/ -- Agnisys, a pioneer and industry leader in Executable Golden Specification Solutions™, is excited to announce its participation in DVCon U.S.. Agnisys will be presenting at two Accellera workshops, focusing on the CDC/RDC interchange format standard and the IP-XACT standard.



NEWS

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Devendra Gupta, Principal Design & Verification Engineer at Agnisys including the most comprehensive solution to chip integration, specially AI chips," said Devendra Gupta, Principal Design & Verification Engineer at Agnisys. "We will also show how our customers can target ASICs or FPGAs based on their design specification. Updates to ispec.ai and smartdatasheet.com will be shown. Be sure to stop by and ask for the winter goodie (while supplies last)."

DVCon U.S. is the premier conference for design and verification engineers, offering a unique platform for industry leaders to come together and share insights, innovations, and best practices. Agnisys, Inc.'s presence at DVCon U.S. underscores its commitment to driving

innovation and standards in the electronic design automation (EDA) and semiconductor

industry.

At DVCon U.S., Agnisys will play a key role in advancing industry knowledge by presenting at two highly anticipated workshops on behalf of the Accellera Systems Initiative:

SoC development automation using IP-

XACT 1685-2022 standard Date: February 27, 2025 Time: 9:00 AM - 10:30 AM

Location: Siskiyou

CDC/RDC Interchange Format Standard

Date: February 27, 2025 Time: 11:00 AM - 12:30 PM

Location: Siskiyou

These workshops will provide attendees with valuable insights into the latest advancements and practical applications of these critical standards, helping streamline design and verification processes across the industry.

Agnisys invites all DVCon U.S. attendees to visit booth #123 to learn more about its innovative solutions.

AGNISYS

SYSTEMS INTERIOR

SOC development automation using IP-XACT 1685-2022 standard

February 27, 2025

9:00 - 10:30

Siskiyou

Agnisys will be presenting a workshop on "SoC development automation using IP-XACT 1685-2022 standard" at DVCon U.S. US on February 27, 2025, as part of the Accellera Systems Initiative workshops.



Agnisys will be presenting a workshop on "CDC/RDC Interchange Format Standard" at DVCon U.S. US on February 27, 2025, as part of the Accellera Systems Initiative workshops.

Exhibits will be open on February 25, 2025 from 1:30 PM until 5:00 PM and February 26, 2025 from 1:00 PM until 5:00 PM. <u>Click here</u> for more information about how Agnisys helps in AI chip design and why top AI hardware companies choose IDesignSpec™.

About Agnisys

Agnisys, Inc., a provider of Electronic Design Automation (EDA) software and methodology services, solves complex front-end design, verification, and validation problems in system chip development. Its certified IDesignSpec™ Suite leverages a golden executable specification to capture and centralize registers, sequences, and connectivity for Intellectual Property (IP) and System-on-a-Chip (SoC) projects. Its intuitive user interfaces and standards-based workflows reduce risk by eliminating development errors while increasing productivity and efficiency through the automatic generation of collateral for the entire project development team. Founded in 2007, Agnisys is headquartered in Boston, Massachusetts, with R&D centers in the

United States and India. Learn more at www.agnisys.com.

About Accellera CDC and IP-XACT Working Groups

The Accellera CDC and IP-XACT Working Groups are committed to advancing standards and best practices in the areas of clock domain crossing (CDC) verification and IP integration using IP-XACT. Through collaboration and industry expertise, the working groups drive innovation and adoption in these critical areas of electronic design.

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