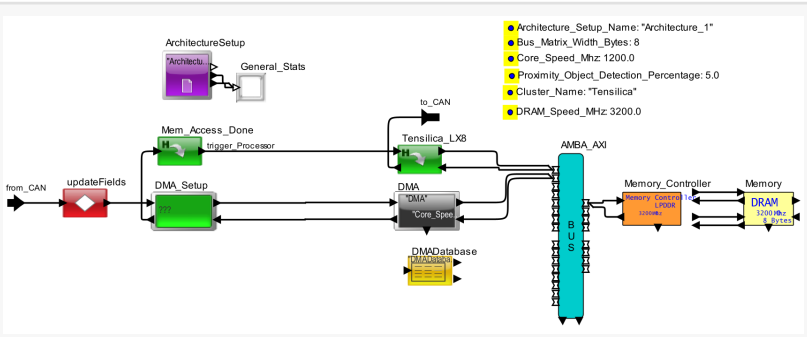
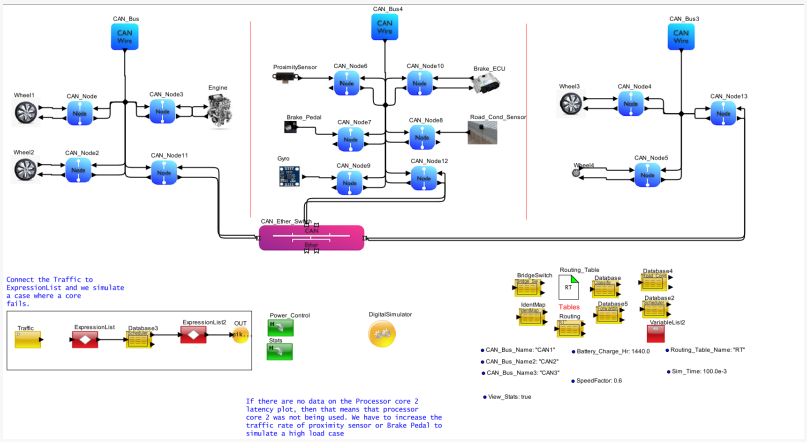
Mirabilis Design Accelerates SoC Development with New System-Level IP Library for Cadence Tensilica Processors

The addition of the Tensilica Xtensa LX7 and LX8 processors expands Mirabilis Design's already comprehensive VisualSim System-Level Processor IP library.



Integrating Tensilic Lx8 into an System-level SoC model



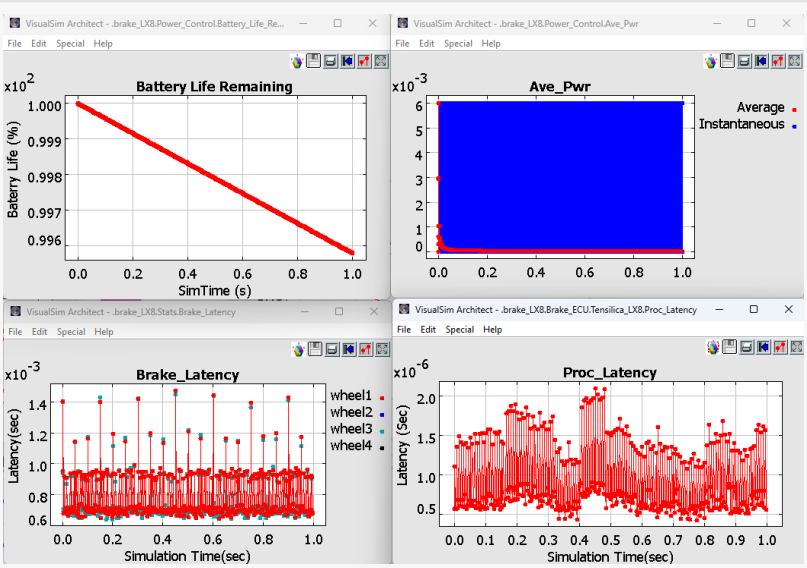
Tensilica SoC used in an ECU that is part of the braking system

SANTA CLARA, CA, UNITED STATES, February 17, 2025 /EINPresswire.com/ -- Mirabilis Design, the industry leader in system-level modeling and architecture exploration, today announces the release of its new system-level IP library for Cadence Tensilica Xtensa LX7 and LX8 processors. This solution enables SoC designers to perform rapid architecture exploration and optimization, helping them make informed decisions at the beginning of the design process.

The Cadence Tensilica Xtensa LX processor platform is known for its configurability, allowing designers to customize the processor cores to optimize for a wide variety of applications. The new Mirabilis VisualSim system-level models of the Xtensa LX7 and LX8 processors allow designers to quickly select the number of cores, optimize the topology of the SoC, conduct regression tests against the target workloads and determine the power and performance improvements of custom instructions.

"To enable Shift-Left, development must truly start at the conceptual phase. With the introduction of Tensilica Xtensa LX7 and LX8 processor models in VisualSim Architect, the SoC architecture team can visualize the system specification early in the design and provide a

platform for collaboration with the end customers to ensure the requirements are met," said Andrea Kroll, director of product marketing for Tensilica platforms in the Silicon Solutions Group at Cadence. "The combined flexibility of the Xtensa LX7 and LX8 processors, together with the early validation provided by VisualSim Architect, allows for a more streamlined design process."



Statistics from the Tensilica Lx8 model during an architecture simulation

Expanding the VisualSim Processor IP Library

The addition of the Tensilica Xtensa LX7 and LX8 processors expands Mirabilis Design's already comprehensive VisualSim System-Level Processor IP library, which supports various processor families such as Arm, RISC-V, x86, PowerPC, and more.

Key Benefits of VisualSim Architect for SoC Designers

Efficient Architecture Exploration: With the system-level models of the Tensilica Xtensa LX7 and LX8 processors built into VisualSim Architect, SoC designers can quickly determine how choices around performance, power consumption, and area size play out, while also easily testing the impact of custom instructions.

Comprehensive System-Level Simulation: VisualSim Architect provides an integrated environment where designers can simulate not only processor cores but also memory subsystems, peripherals, and interconnects, giving a complete performance overview of the entire SoC.

Digital Twin Technology: Designers can validate performance, power consumption, and functional requirements before committing to hardware, ensuring that the final design meets its specifications.

Accelerated Time-to-Market: By offering early-stage architectural exploration and simulation, VisualSim Architect significantly reduces the need for hardware iterations.

Availability

The Cadence Tensilica Xtensa LX7 and LX8 processor system-level models are available now as part of the VisualSim System-Level Processor IP library. This library requires VisualSim Architect

version 2420. The product runs on Linux, Windows and Mac.

For more information visit MirabilisDesign.com

About Mirabilis Design Inc.

Mirabilis Design is a Silicon Valley software company, providing software and training solutions to identify and eliminate risk in the product specification, accurately predicting the human and time resources required to develop the product, and improve communication between diverse engineering teams. VisualSim Architect combines Intellectual Property, system-level modeling, simulation, environment analysis and application templates to significantly improve model construction, simulation, analysis and RTL verification. The environment enables designers to rapidly converge to a design which meets a diverse set of interdependent time and power requirements. It is used very early in the design process in parallel with (and as an aid to) the written specification and before an implementation (for example, RTL, software code, or schematic) of the product.

For media inquiries, please contact: info@mirabilisdesign.com

Deepak Shankar
Mirabilis Design Inc
+1 408-245-8992
dshankar@mirabilisdesign.com
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X
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