

# 2D Graphene Interconnects for CMOS and Integrated Circuits

*Inventor Bellezza Has Several US Patents for Fusing Circuits Using Low Temperatures Within The Thermo Budget of CMOS Chips, It is a Single Step Process.*

PARKESBURG, PA, UNITED STATES, March 20, 2025 /EINPresswire.com/ -- Anthony Paul Bellezza has pioneered a novel 2D Graphene fusion process for semiconductor assembly, operating at low temperatures, which holds the potential to revolutionize CMOS chip manufacturing. This innovative process addresses the longstanding challenge of integrating Graphene into circuits, a problem that has persisted since its discovery in 2004.

**Innovative Graphene Fusion Process:** My method enables the utilization of 2D Graphene as an interconnect material in semiconductor circuits, forming a low-resistance, metallurgical bond with the substrate. This advancement will lead to the production of faster and more efficient computers by replacing traditional copper circuits, which are approaching their physical limitations.

Bellezza Technologies brings 2D Graphene into mainstream of semiconductor assembly processes.

Anthony Paul Bellezza the inventor of a 2D Graphene fusion process being used for CMOS Chip assembly processes, that fuses interconnects at temperatures within the thermal budget of the chip below 400 degrees C. and can work at temperatures as low as 200 degrees C. The interconnect electrical resistance is almost undetectable; this will allow faster computers to be produced that operate at lower temperatures as Graphene is also an excellent disperser of heat produced by the chips. My patent process will extend Moor's law and will in time eliminate copper circuits that will be replaced by environmentally safer Graphene as the Copper circuit size is now at the limit. Thinner, copper micro circuits increase electrical resistance.

Scientist and Engineers have been trying to use Graphene in semiconductor circuits since Andre Geim and Konstantin Novoselov's Graphene discovery in 2004. Graphene is hundreds of times more conductive than copper. The biggest problem has been that Graphene cannot be soldered and does not bond well at low temperatures with any other metals used in circuits. It is the world's best diffusion barrier that prevents oxidation and metal migration in circuits. My fusion process is the only process in the world that can use 2D Graphene for circuit interconnects at low temperature assembling of CMOS Chips. This is done by changing the crystalline structure of the

substrate metal which is Iron/Nickel plating. The substrate is prepared by physically rolling or cryogenically treating for only seconds to form Martensite crystals that will absorb Carbon Graphene when heated. This type of process has been used for several hundred years in heat-treating Carbonization of Steel, but I'm the first in the world to use this heat-treating process for microelectronic circuits. The fusion created is a true metallurgical union as the Graphene becomes an Alloy fused to the substrate and CMOS Chips. The interface has very low electrical resistance that increases the speed of the circuit. My process can be used for all circuits in Semiconductors. The Carbon Graphene properties are now pivotal and the best for fusing these interconnects.

I have researched the use of this type of fused interconnects in my other patents found on my Web Site. The solderless Thermoelectric Generator was the start of this research in 2007 now patent US10,756,248 followed by patent US11,380,833. I received two granted fusion patents in 2018 and 2021. My fusion patents US10,937,940 and US10,096,761 are the basis of my current work with several more fusion patent applications to be filed soon.

In 2018 when patent US10,096,761 was granted, I sent it out to a few University Engineering departments for their review and comments. Unfortunately, I received no direct response. I was hoping for positive response from the University, but received none.

My patent process will bring 2D Graphene into the main stream of Integrated Circuits for generations to come. I will continue to research improvements in my process.

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