

Agnisys Ignites DAC 2025 with IDesignSpec Suite v9, IDS-FPGA Launch, AI² and IDS-Integrate Enhancements.

Agnisys showcases next-generation EDA solutions at DAC 2025, including IDesignSpec Suite v9, IDS-FPGA Launch, AI² and IDS-Integrate Enhancements.

BOSTON, MA, UNITED STATES, June 18, 2025 /EINPresswire.com/ -- Agnisys, the pioneer and industry leader in Golden Executable Specification Solutions™, is excited to announce its exhibition at [DAC 2025](#), taking place in San Francisco, CA. Visitors can meet the Agnisys team at Booth #2622 on the second floor to explore the latest advances in design automation, embedded systems, and standards-based innovation.



NEWS

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“

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Anupam Bakshi, Founder and CEO of Agnisys, Inc.

At the forefront of the event, Agnisys will showcase Version 9 of its flagship IDesignSpec (IDS) Suite, delivering powerful new features including:

- A simplified user experience with an improved interface
- Enhanced [IDS-Integrate](#) with Git and Physical Design awareness, and support for the latest industry standards in CDC, UPF, SDC, and IP-XACT 2022
- Full VHDL support, with updates to IDS-Verify and IDS-Validate
- Java and C/C++ APIs for custom plugin development
- Complete IP portfolio of bridges, crossbars, and decoders

Agnisys is unveiling IDS-FPGA, a newly repackaged version of the IDesignSpec Suite tailored specifically for FPGA developers. IDS-FPGA enables users to create register maps and programming sequences directly within their FPGA design environment, generating design,

verification, and validation collateral with just a click. The tool seamlessly integrates with leading FPGA toolchains for streamlined development.

Another highlight at DAC 2025 is the introduction of AI² (Agnisys Inc. Artificial Intelligence), a collaborative [AI](#) platform that significantly reduces the time required to build testbenches and tests. This groundbreaking capability signals a major leap toward the future of automated and intelligent verification.



The poster features logos for Agnisys, Accellera, and The Chips to Systems Conference. The main title is 'Engineering Special Session' in large blue font, followed by 'CDC-RDC Inter-operable Collateral Standardization' in black. Below this, the date and time are listed: 'Date & Time: Monday, June 23, 2025 / 10:30am - 12:00pm PDT' and the location: 'Visit: 2008, Level 2'. The background of the poster shows a hand holding a small electronic component over a circuit board.

Engineering Special Session on CDC-RDC Inter-operable Collateral Standardization at DAC 2025.

Engineering Special Session

Agnisys, along with other industry experts, will present an Engineering Special Session focused on CDC-RDC collateral standardization on behalf of Accellera:

Title: CDC-RDC Inter-operable Collateral Standardization

Date: Monday, June 23, 2025

Time: 10:30 AM – 12:00 PM PDT

Location: Room 2008, Level 2

This session will address the need for standardized, interoperable data for Clock Domain Crossing (CDC) and Reset Domain Crossing (RDC) analysis. Attendees will learn how abstract models and tool-independent formats improve hierarchical signoff, enhance design accuracy, and drive seamless tool integration.

Booth Activities

Stop by Booth #2622 to:

- See live demos of IDesignSpec, IDS-Integrate, IDS-FPGA, and AI²
- Meet Agnisys R&D experts and leadership
- Collect a rare gift and participate in a raffle to win an exciting electronic kit

“At DAC 2025, we’re not just demonstrating tools—we’re showing the future of intelligent, automated design,” said Anupam Bakshi, Founder and CEO of Agnisys, Inc. “From abstract model standards to AI-powered test creation, Agnisys is shaping a more interoperable, efficient, and innovation-driven hardware design ecosystem.”

About Agnisys

Agnisys is a provider of Electronic Design Automation (EDA) software and methodology services, solving complex front-end design, verification, and validation problems in system chip

development. Its ISO certified IDesignSpec™ Solution Suite leverages a golden executable specification to capture and centralize registers, sequences, and connectivity for Intellectual Property (IP) and System-on-a-Chip (SoC) projects. Its intuitive user interfaces and standards-based workflows reduce risk by eliminating development errors while increasing productivity and efficiency through the automatic generation of collateral for the entire project development team. Founded in 2007, Agnisys is headquartered in Boston, Massachusetts, with R&D centers in the United States and India. Learn more at www.agnisys.com.

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