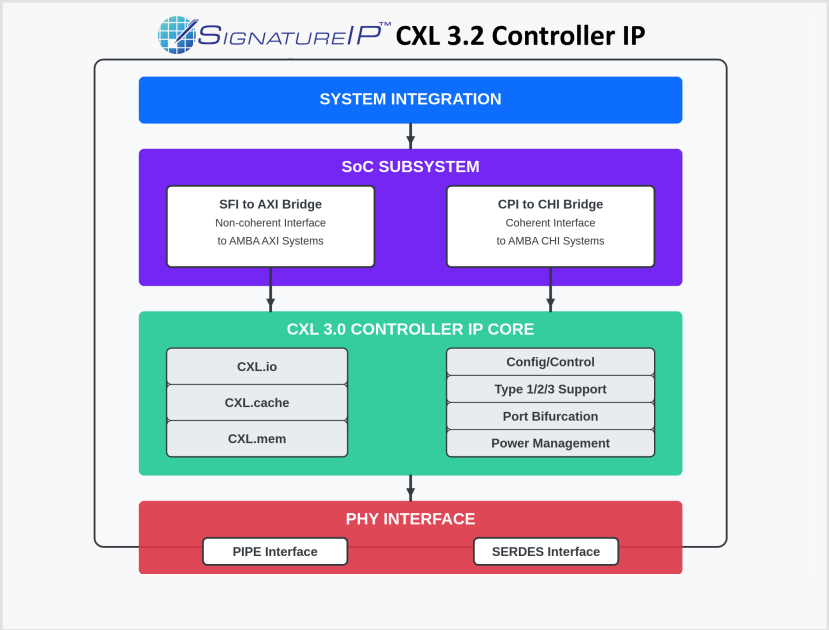
SignatureIP Unveils Industry-Leading CXL 3.2 Solution for High-Performance Computing

New CXL 3.2 IP and Flex Bus Port Technology Delivers Enhanced Performance for Next-Generation Data Center, AI, and HPC Applications



MILPITAS, CA, UNITED STATES, June 23, 2025 /EINPresswire.com/ -- SignatureIP, a leading provider of interconnect and interface solutions for high-performance systems, announces the launch of its latest CXL 3.2 solution. This next-generation technology introduces advanced multi-protocol capabilities, supporting both 68B and 256B flit modes with data rates up to 64 GT/s to revolutionize data center, AI, and high-performance computing (HPC) applications.

The Power of CXL 3.2
CXL (Compute Express Link) is a versatile, high-speed interconnect standard built on PCIe's electrical foundation, delivering powerful I/O, memory, and caching protocols to address the demanding requirements of modern computing systems. SignatureIP's implementation provides full backward compatibility with CXL 1.1 and 2.0 while introducing CXL 3.2's advanced features, including:

- CXL.io: Provides I/O semantics similar to PCIe, enabling configuration, memory, and I/O transactions with enhanced features such as vendor-defined messaging for power management and error notification.
- CXL.cache: Supports coherent caching protocols with three dedicated channels (Request, Response, and Data) in each direction, optimized for high-throughput, low-latency coherent transactions between CPUs, GPUs, and memory devices.
- CXL.mem: Delivers memory access semantics supporting HDM-H (Host-only Coherent), HDM-D (Device Coherent), and HDM-DB (Device Coherent using Back-Invalidation) models, enabling efficient memory sharing and pooling across devices.

Introducing Flex Bus Port Technology

SignatureIP's new Flex Bus Port technology is a game-changer for systems requiring protocol flexibility. The Flex Bus port dynamically supports both PCIe and CXL protocols, offering:

- Dynamic Protocol Selection: During link training, the system determines whether to operate in PCIe mode or CXL Flex Bus mode based on connected device requirements.
- Multiple Flit Modes: Support for both 68B and 256B flit modes, with the latter offering latency-optimized options for performance-critical applications.
- Comprehensive Device Type Support: Compatible with all CXL device types (Type 1, 2, and 3), providing maximum flexibility for system architects.
- High-Performance Implementation: Supporting up to 64 GT/s with PAM-4 signaling, leveraging PCIe 6.0 physical layer with CXL's enhanced reliability features including CRC and FEC.

Advanced CXL Controller IP Architecture

SignatureIP's CXL Controller IP features a sophisticated microarchitecture that includes:

- Unified Transaction and Link Layers: Optimized implementation of CXL.cm layers with efficient credit-based flow control mechanisms.
- Intelligent ARB/MUX Layer: Advanced arbitration between CXL.io and CXL.cm traffic with programmable weighting to optimize performance for specific workloads.
- Enhanced Physical Layer: Flex Bus physical layer supporting multiple link widths (x1, x2, x4, x8, x16) and speeds, with seamless support for PCIe retimers and form factors.
- Power Management: Comprehensive power management capabilities including ASPM L1 and L2 support with sophisticated state management for optimal energy efficiency.
- Standardized CPI Interface: Implementation of the Compute Express Link Protocol Interface (CPI) for seamless integration with CXL devices.

Unlock the Potential of CXL 3.2 with SignatureIP

SignatureIP's CXL 3.2 solution is designed for cutting-edge data center, AI, and HPC applications, enabling developers to take full advantage of the flexibility and performance offered by CXL. With its support for multiple device types, high-performance interconnects, and seamless PCIe integration, SignatureIP's CXL solution is ideal for building scalable, high-performance systems. "Our CXL 3.2 IP represents a significant advancement in interconnect technology," said Purna Mohanty, CEO at SignatureIP. "Our customers can now design heterogeneous RISC-V compute and IO subsystems for their chiplet SoCs leveraging SignatureIP components – Coherent and Non-coherent NoC, PCIe, CXL, System IPs”

About SignatureIP

SignatureIP is building the industry's first web-based Network-on-Chip (NoC) design and development tools, and a portfolio of high-performance NoC Interconnect IP and High-Speed Interface (PCIe, CXL, UCIe) IPs for developers of AI/ML, HPC and other systems-on-chip (SoCs).

SignatureIP offers the industry's first web-based, fully customer-configurable "DIY" NoC development tool for both monolithic and chiplet-based SoCs that lowers the entry barrier for SoC architects and developers. The company also offers the lowest-power, highest-performance PCIe Gen6 and CXL 3.2 IPs on the market based on a ground-up fresh design without the legacy overhead of existing competitors. SignatureIP was founded in 2021 and is based in Milpitas, California. See: https://www.signatureip.ai/.

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