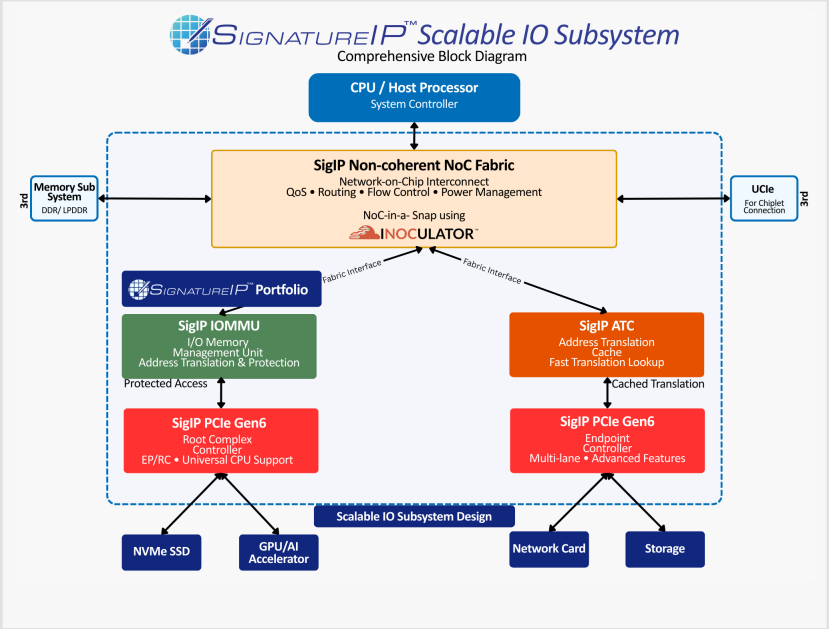
SignatureIP Achieves PCI-SIG® PCIe® 5.0 Certification, Joining Elite Group on Official Integrators List

Next-Generation NoC Pioneer Demonstrates Industry-Leading PCIe Controller IP and Scalable IO Subsystems on Siemens Veloce proFPGA CS Platform



MILPITAS, CA, UNITED STATES, September 4, 2025 /EINPresswire.com/ -- SignatureIP, the pioneer of next-generation Network-on-Chip (NoC) and Interface subsystem solutions, just announced that its PCIe Controller IP has successfully passed PCI-SIG® compliance testing and has been added to the official PCI Express® 5.0 Integrators List.

Additionally, running the IP on Siemens' industry-leading Veloce™ proFPGA CS hardware, verifies the scalability and flexibility of SignatureIP's complete IO Subsystem solutions.

Purna Mohanty, CEO of SigntureIP, said that "Achieving PCI-SIG certification for PCIe 5.0 represents a significant validation not just of our engineering excellence but also our commitment to delivering cutting-edge connectivity solutions. SignatureIP PCIe 6.2 Controller incorporates the the performance features configurable based on the system requirement, and is architected for deployment in a broad spectrum of applications in ASIC and FPGA. By using Siemens' Veloce proFPGA CS, we've demonstrated not just PCIe compliance but also the full capabilities of our connectivity IPs in scaling IO Subsystems. This approach accelerates our customers' path to silicon success."

Siemens' Veloce proFPGA CS enabled SignatureIP to demonstrate:

- PCIe 6.2 Compliance with backward compatibility: Full specification compliance
- NoC Scalability: Real-world demonstration of Network-on-Chip performance
- IO Subsystem Integration: Demonstrating comprehensive IO connectivity solutions with

scalable architecture with SignatureIP System-level IPs that includes System-level Cache, IOMMU, Proxy Cache Designs.

"It is exciting to see IP providers like SignatureIP take full advantage of the unique capabilities of Veloce proFPGA CS to achieve PCIe 5.0 certification. It demonstrates the convergence of two critical technologies for next-generation computing. SignatureIP's PCIe/CXL interface IP delivers the high-bandwidth, scalable connectivity that modern systems require for connecting CPUs, GPUs, and memory—the fundamental building blocks of an AI infrastructure. The advanced FPGA-based prototyping capabities of Veloce proFPGA CS allow joint customers to not only integrate the IP into their designs but also verify functionality in an at-speed prototyping environment. " said Juergen Jaegar, Director, Prototyping Product Strategy, Siemens Digital Industries Software.

Technical Excellence and Innovation

SignatureIP's PCIe Controller IP, stands out in the market with several key differentiators:
- Modular Architecture: Designed from scratch with a clean, modular approach allowing customers to add or remove features to meet exact requirements
- Superior Performance: Achieves outstanding operating frequency of up to 1 GHz for Gen 6 data rates while maintaining full backward compatibility from Gen 1 to Gen 6
- Minimal Footprint: No legacy code overhead ensures industry-leading small area implementation
- Built-in Debug Features: Integrated trace and debug capabilities accelerate customer time-to-market

Comprehensive Solution Offering

SignatureIP specializes in building custom IO subsystems based on its cloud-active iNoCulator tool based NoC and PCIe/CXL Controller IPs. The company delivers the solution as synthesizable RTL along with:

- Complete sample testbenches and tests for easy implementation
- Scripts for simulation, synthesis, and timing closure
- Comprehensive documentation for seamless integration
- Full support for power management including clock gating and power gating capabilities
- Proven demonstration on the Veloce proFPGA and Veloce proFPGA CS platforms for FPGA-based prototyping

Platform Validation and Customer Benefits

Veloce proFPGA CS for certification and demonstration provides customers with:

- Risk Reduction: Pre-validated IP on industry-standard prototyping platform

- Faster Time-to-Market: Proven interoperability and compliance
- System-Level Validation: Complete subsystem demonstration beyond just interface IP
- Scalability Proof Points: Demonstrated scaling of compute and IO resources

About SignatureIP

SignatureIP is the pioneer of the next-generation NoC and Interface IP based solutions. Founded in 2021 to develop advanced Network-on-Chip (NoC) solutions that form the basis for a full SOC platform design. SignatureIP features 120+ person-years of engineering leadership in interconnect, networking, data center, storage, and connectivity IP, from specification to production. The company's team has extensive engineering expertise in interconnects, interfaces, bus protocols, CPUs, and AI processing. SignatureIP headquarters is located in Milpitas, California.

For more information about SignatureIP's PCIe, CXL and NoC solutions, visit https://www.signatureip.ai

Editor's Notes:

- The PCI-SIG Integrators List represents products that have successfully completed rigorous compliance testing at official PCI-SIG workshops, ensuring interoperability across the PCIe ecosystem.
- PCIe 7.0 specification doubles the bandwidth of PCIe 6.0, delivering 128 GT/s raw bit rate and up to 128 GB/s of bidirectional bandwidth in x16 configurations.
- PCIe 6.0 specification doubles the bandwidth of PCIe 5.0, delivering 64 GT/s raw bit rate and up to 128 GB/s of bidirectional bandwidth in x16 configurations.
- PCIe 5.0 specification doubles the bandwidth of PCIe 4.0, delivering 32 GT/s raw bit rate and up to 128 GB/s of bidirectional bandwidth in x16 configurations.
- SignatureIP's achievement can be verified on the official PCI-SIG Integrators List at: https://pcisig.com/developers/integrators-list
- The Siemens proFPGA CS Platform provides a comprehensive FPGA-based prototyping environment for complex SoC designs, enabling pre-silicon validation and software development.

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