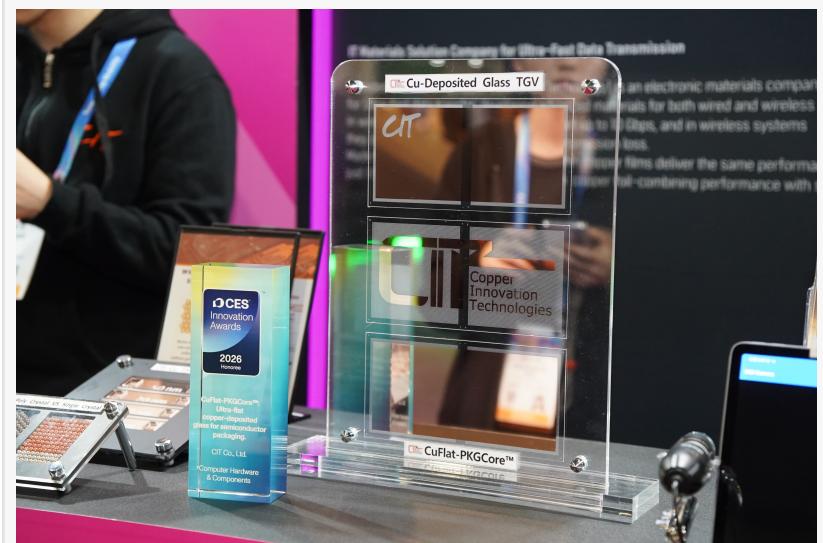


CIT Showcases Ultra-Flat Copper Technology, Two-Time CES Innovation Award Winner, at CES 2026

CIT Targets Global AI Semiconductor Market with CuFlat PKGCore

LAS VEGAS, NV, UNITED STATES, January 20, 2026 /EINPresswire.com/ -- CIT (CEO Seung Jeong) announced its participation in CES 2026, the world's largest IT and consumer electronics exhibition, held in Las Vegas beginning January 6 (local time), where it unveiled its ultra-flat semiconductor packaging solution, CuFlat Package Core (CuFlat-PKGCore).

CIT is an advanced materials and packaging technology startup specializing in next-generation copper processing technologies. After earning a CES Innovation Award last year for its transparent antenna "Dolphin," which features ultra-thin copper circuitry formed using the company's proprietary Atomic Sputtering Epitaxy (ASE) technology, CIT once again received a CES Innovation Award in 2026. This year's recognition came through the application of ASE to glass substrates for semiconductor packaging with CuFlat-PKGCore, marking two consecutive years of CES Innovation Award honors.



CIT's CuFlat Package Core (CuFlat-PKGCore) on display at CES 2026, along with the trophy of CES Innovation Award 2026



A scene from CIT's booth at Busan Pavilion at CES 2026

The back-to-back awards highlight CIT's transition from a materials-focused startup to a

company specializing in advanced AI semiconductor packaging technologies, while also validating its technology as a scalable and sustainable materials solution suitable for next-generation semiconductor manufacturing.

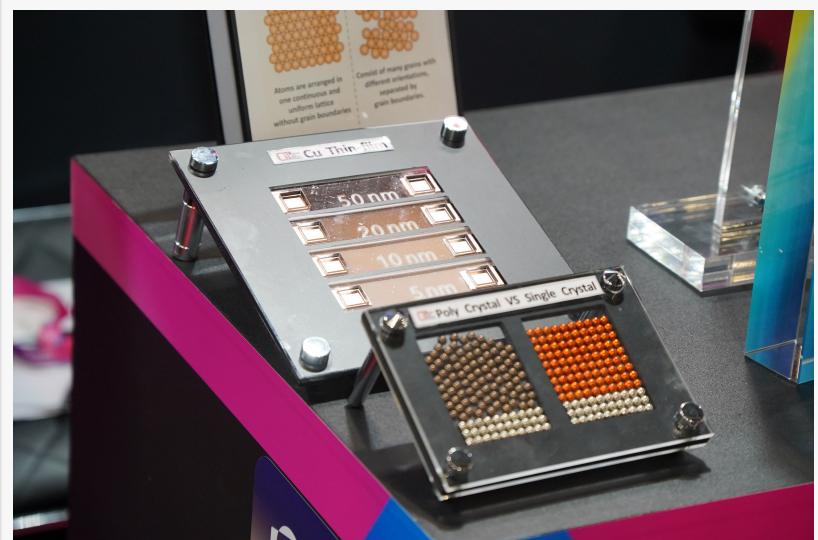
ASE, the core technology behind CIT's consecutive awards, is a copper deposition process that stacks copper atoms layer by layer on insulating substrates, forming a single-crystal structure without the use of adhesives. This method allows precise control of copper thickness and surface roughness at the nanometer scale, enabling stable, high-quality copper formation on glass substrates. In this area, conventional technologies have faced significant limitations. The scientific validity of ASE has also been recognized academically, with related research published in *Nature* in May 2022 and later featured in *Advanced Materials*, a leading international materials science journal.

The CES 2026 Innovation Award-winning CuFlat-PKGCore applies ASE technology to glass substrates used in semiconductor packaging. By achieving surface roughness below 3 nanometers, the solution delivers a level of flatness more than 200 times smoother than HVLP4 copper foil, which is regarded as one of the flattest copper materials currently used in AI accelerator package substrates.

This ultra-smooth copper surface significantly reduces signal scattering and transmission loss in high-frequency environments. As a result, CuFlat-PKGCore supports stable signal integrity and improved power efficiency in packaging for AI accelerators, high-bandwidth memory (HBM), and network chips that handle high-speed, high-frequency signals. CIT noted that the material also enables finer patterning and high-density routing, offering greater design flexibility for semiconductor package engineers.

CuFlat-PKGCore further demonstrates strong thermal stability. While conventional copper materials typically oxidize and experience performance degradation at temperatures near 100°C, CuFlat-PKGCore maintains structural integrity without oxidation or delamination even at temperatures up to 250°C. This characteristic makes it well-suited for high-performance AI accelerator packages, where thermal load and reliability are critical concerns.

From a sustainability and process-efficiency perspective, CIT emphasized that CuFlat-PKGCore is produced from 100 percent recycled copper scrap and a dry ASE deposition process that



Cu Thin film samples and comparison model of polycrystal and single-crystal structures on display

eliminates the need for seed layers and chemical-mechanical polishing (CMP). Compared with conventional copper processing, this approach reduces carbon emissions by approximately 95 percent and minimizes chemical wastewater by avoiding electroplating.

With its ultra-flat copper-on-glass structure, CuFlat-PKGCore is positioned to meet the stringent design and performance requirements of the AI semiconductor industry, supporting the computational power and memory bandwidth demanded by next-generation devices. Given the growing adoption of glass substrates for cores, interposers, and other advanced package architectures, the technology is also expected to gain traction as a platform for high-density packaging, including 2.5D and 3D packaging.

CIT is currently conducting proof-of-concept projects with leading companies in the United States and Japan, including glass substrate manufacturers, transparent antenna developers, and semiconductor equipment firms, while also pursuing joint development programs for AI accelerator substrates with major domestic corporations. As the company expands its global collaboration network across semiconductor hubs in Korea, the United States, Japan, and Taiwan, it plans to actively promote the capabilities and industrial impact of its ASE-based technologies through continued engagement at CES 2026.

Seung Jeong, CEO of CIT, said, "With two consecutive CES Innovation Awards, our ASE technology has been recognized globally for its technical maturity and future value. CES 2026 will catalyze new collaborations and market opportunities. By delivering the stability, energy efficiency, and environmental sustainability required in the AI semiconductor era, we aim to establish a new standard in the global semiconductor packaging market."

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