YorChip and Partners launch Physical AI Chiplet Ecosystem (P.A.C.E.)

YorChip announces two key initiatives as part of a comprehensive effort to jumpstart Chiplet adoption for the Physical AI market.

SAN RAMON, CA, UNITED STATES, February 17, 2026 /EINPresswire.com/ -- – YorChip announces two key initiatives as part of a comprehensive effort to jumpstart Chiplet adoption for the Physical AI market.
The first is to offer a free Multi Project Wafer (MPW) use license of its UCIe

PHY for system/ASIC customers to develop and prototype their own custom Chiplets at the 28nm TSMC node.

The second is the launch of the Physical AI Chiplet Ecosystem (PACE) with multiple semiconductor IP companies to co-develop interoperable and re-useable PACE Chiplets with system/ASIC customers to save them from having to develop their own common Chiplets - saving them millions of dollars in duplicative IP license fees, redundant Non-Recurring Engineering (NRE) costs, and additional millions of dollars in mask costs. This will enable system customers to focus on their own custom Chiplet design and leverage PACE chiplets to get to market faster and at much lower costs.

> Now we are launching the PACE ecosystem with a broad range of partners to co-develop re-useable Chiplets to smash through the Chiplet Wall. Free MPW use of our PHY at 28nm TSMC for designers"
>
> *Kash Johal*

"Splitting a complex, monolithic design into multiple Chiplets makes sense technically, but as a practical matter, there is huge Chiplet Wall – high development costs and long time-to-market," stated Kash Johal CEO of YorChip. "This has stopped wider Chiplet adoption in its tracks, at YorChip we have developed a Universal UCIe PHY optimized for lowest power and area cost needed for Physical AI. The PHY is 100% digital and supports any Foundry and node from 28nm through to 2nm.Now we are launching the PACE ecosystem with a broad range of partners to co-develop re-useable

Chiplets to smash through the Chiplet Wall. Free MPW use of our PHY at 28nm TSMC for system/ASIC companies will enable development of their own custom Chiplets inexpensively and leverage external PACE Chiplets."

"Memory access and bandwidth are critical for todays AI inference developers and we are excited to join the PACE ecosystem and offer our LPDDR5 and LPDDR4 silicon proven PHY and controller IP for PHYSICAL AI Chiplets", stated Mo Tamjidi, CEO of Dolphin Technology."We are supporting YorChip's development of a scalable memory subsystem Chiplet for PHYSICAL AI customers. We also plan to license our Memory PHY and controller IP for customers to develop their own Chiplets as needed by customers."

"QuickLogic is excited to join the PACE program to enable eFPGA-based Chiplets for Physical AI. With fast time-to-market as a key requirement, eFPGA chiplets deliver ultra-low power, security, and immediate post-silicon flexibility — including field updates when needed. Physical AI systems rely on diverse sensor inputs such as audio, vision, location, and radar, making eFPGAs ideal for sensor fusion and pre-processing ahead of compute and AI engine Chiplets," stated Brian Faith CEO of QuickLogic. "Building on our licensable eFPGA IP, QuickLogic plans to offer finished PACE Chiplets ranging from 5K to 100K+ LUTs, supporting process nodes from 28nm to advanced technologies as the ecosystem evolves."

"We are pleased to join the PACE program and work together to enable MRAM based solutions for Physical AI. We provide robust high-performance non-volatile memory to assist securing PACE Chiplets for secure boot, weight storage, code storage, and lifecycle management solutions," stated Sanjeev Aggarwal, President and CEO of Everspin Technologies. "Physicals AI requires low latency local compute and non-volatile, LPDDR MRAM technology from Everspin is ideal for this market. We plan to provide licensable IP and finished Chiplets based on customer feedback and as demand unfolds."

"We are pleased to support the PACE program and collaborate to advance on-device and always-on AI solutions. Blumind's compute-in-transistor technology delivers ultra-low power and latency AI inferencing required for the next generation of intelligent devices and robotics,"stated Niraj Mathur CEO of Blumind. "We plan to provide licensable IP and future PACE compatible Chiplets based on customer feedback as market demand for Physical AI unfolds."

Additional PACE partners will join and provide IP and design services including:

 Sofics from Belgium to help support YorChip's PHY migration to all TSMC Nodes
 GSOC from Israel to provide management, compute and Chiplet management IP
 Crypto Quantique to provide Root of Trust and PUF IP for PACE Chiplets and customers
 Chip Interfaces to provide JESD204, Interlaken and UCIe IP for PACE Chiplets and customers

Customers can join and get more information on all the partners and updates at

PaceChiplets.com.

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