EINPRESSWIRE

Sarcina Launches UCIe-A/S Packaging IP to Accelerate Chiplet Architectures

Sarcina launches UCIe-A/S Packaging IP, enabling high-performance, scalable chiplet interconnects with reduced complexity and faster time-to-market.

PALO ALTO, CA, UNITED STATES, April 9, 2026 /EINPresswire.com/ -- Sarcina Technology today announced the availability of its UCIe-A/S Packaging IP, a high-performance die-to-die (D2D) interconnect solution implemented at the package level—over interposer or substrate. The solution is designed to meet the rapidly growing demands of chiplet-based system architectures across high-performance computing (HPC), artificial intelligence (AI), data center infrastructure, next-generation networking platforms, and co-packaged optics (CPO).

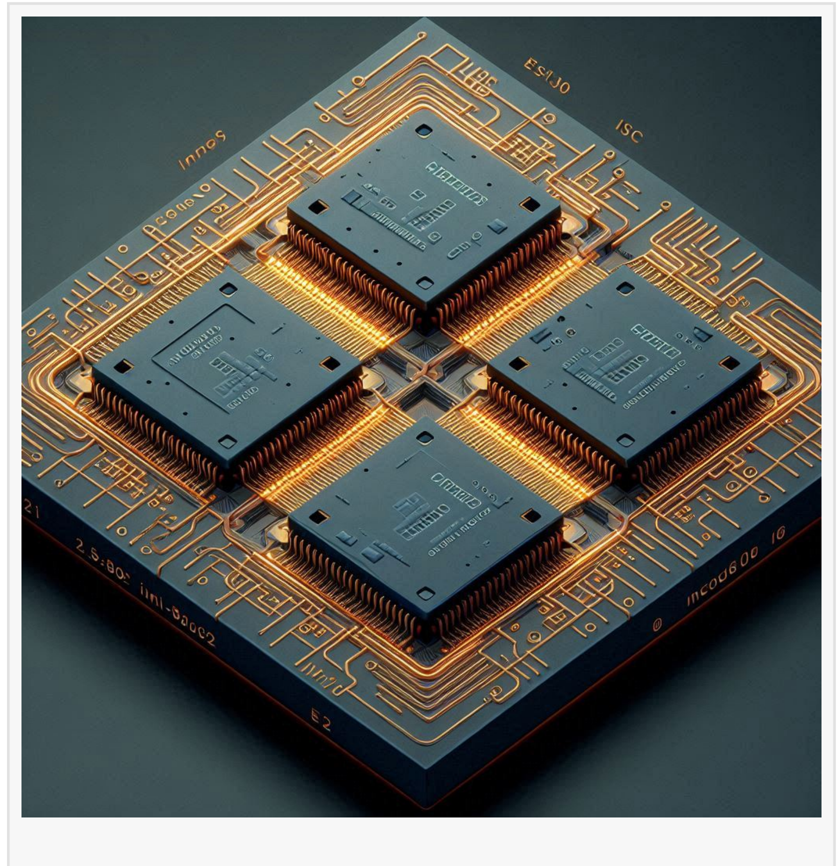
> We're empowering our customers to leverage UCIe connectivity at the package level—reducing complexity while accelerating time-to-market."
> *Eric Gunn, VP of Sales, Sarcina*

Unlike traditional silicon-based interface IP, Sarcina's UCIe-A/S Packaging IP targets the physical D2D interconnection layer within the package. This approach enables customers to achieve high-performance, standards-compliant connectivity without the need to develop complex packaging solutions in-house.

Sarcina's UCIe-A/S Packaging IP delivers strong performance across critical design dimensions, including signal integrity (SI), power integrity (PI), routing efficiency, silicon utilization, and manufacturability—key enablers for modern heterogeneous integration.

The UCIe-A Packaging IP is optimized for efficiency, utilizing a minimal number of copper redistribution layers (RDL) while supporting a 64-bit D2D interconnect using a standard UCIe-A module. Its architecture aligns interconnect width with the die bump "beachfront," allowing multiple modules to be placed along the die edge without increasing module-to-module spacing.

This design maximizes silicon utilization, reduces die area overhead, and lowers overall system cost.



Fully compliant with the UCIe 2.0 standard, the UCIe-A Packaging IP supports data rates of up to 32 GT/s, with channel simulations demonstrating strong eye margin performance.

Sarcina's UCIe-S Packaging IP is designed for scalability and flexibility. Beginning with a 16-bit configuration, bandwidth can be doubled to 32 bits without increasing beachfront width by stacking modules behind the primary interface. This modular approach scales seamlessly to higher bandwidth configurations—64, 128, 256 bits, and beyond—along the die edge, enabling increased performance without compromising layout efficiency.

At the package level, the UCIe-S architecture confines routing within the D2D region, enabling tighter module placement and minimizing substrate resource consumption. This optimization frees valuable routing area for critical functions such as power delivery. Simulation results demonstrate robust signal integrity, with extrapolated eye contours remaining outside the mask at a BER of 1E-15, ensuring reliable operation at full 32 GT/s data rates. The technology is currently undergoing silicon qualification, reinforcing Sarcina's commitment to delivering production-ready, high-reliability solutions.

Engineered for scalability, efficiency, and robustness, Sarcina's patented UCIe-A/S Packaging IP reduces system complexity while enabling high-performance interconnect in advanced packaging environments.

Offered as part of Sarcina's comprehensive advanced packaging design and production services, the UCIe-A/S Packaging IP enables customers—from leading semiconductor companies to emerging AI startups—to accelerate development timelines, reduce design risk, and achieve first-pass success. Flexible licensing options are available to meet diverse customer requirements.

"The launch of our UCIe-A/S Packaging IP marks a significant step forward in enabling scalable, high-performance chiplet systems," said Eric Gunn, VP of Sales at Sarcina. "We're empowering our customers to leverage UCIe connectivity at the package level—reducing complexity while

accelerating time-to-market.”

For licensing inquiries or more information, please contact:
Eric.Gunn@sarcina-tech.com

About Sarcina
Sarcina is a leader in advanced packaging design and production services, delivering innovative solutions that enable next-generation semiconductor systems. Focused on performance, scalability, and integration, Sarcina helps customers—from startups to industry leaders—bring complex chiplet-based designs to market faster, more efficiently, and with greater confidence.

Eric Gunn
Sarcina Technology LLC
Eric.Gunn@sarcina-tech.com
Visit us on social media:
LinkedIn

This press release can be viewed online at: https://www.einpresswire.com/article/904582960

EIN Presswire's priority is source transparency. We do not allow opaque clients, and our editors try to be careful about weeding out false and misleading content. As a user, if you see something we have missed, please do bring it to our attention. Your help is welcome. EIN Presswire, Everyone's Internet News Presswire™, tries to define some of the boundaries that are reasonable in today's world. Please see our Editorial Guidelines for more information.
© 1995-2026 Newsmatics Inc. All Right Reserved.