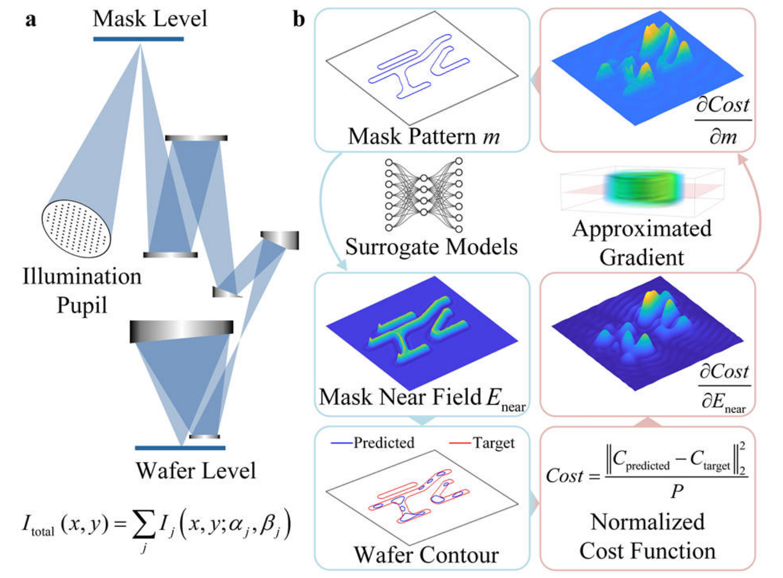
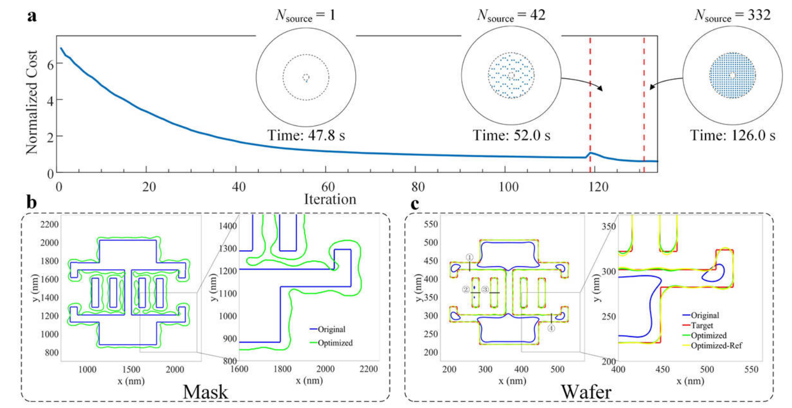
Full-chip EUV Curvilinear Mask Optimization

GA, UNITED STATES, May 12, 2026 /EINPresswire.com/ -- Prof. Shiyuan Liu's team from Huazhong University of Science and Technology has reported a full-chip EUV curvilinear mask optimization framework that integrates deep learning with gradient-based inverse optimization. This framework achieves an estimated speedup of four orders of magnitude over conventional FDTD methods while preserving accuracy, thereby enabling full-chip EUV mask optimization within a practical runtime. Doctoral student Pinxuan He is the first author of this paper, and Prof. Shiyuan Liu and Dr. Jiamin Liu are the co-corresponding authors. Prof. Honggang Gu, Dr. Song Zhang, Prof. Qi Xia, and Prof. Hao Jiang also contributed to this research.



Schematic of EUV lithography and the proposed mask optimization framework



Mask optimization results and accuracy verification on a typical BigMaC pattern

Lithography stands as one of the core processes in advanced integrated circuit (IC) manufacturing, where exposure precision directly determines the critical dimensions (CDs) and performance of chips. As semiconductor technology advances toward advanced nodes, extreme ultraviolet (EUV) lithography has become the key technology for high-end chip mass production. Mask optimization (MO), which iteratively modifies mask patterns to compensate for imaging distortions induced by optical proximity effects and thick mask effects, is essential to guarantee pattern fidelity and to enlarge process windows.

Compared with deep ultraviolet (DUV) lithography, EUV lithography exhibits significantly enhanced thick mask effects, demanding high-precision electromagnetic models and thus drastically increasing computational costs. Meanwhile, curvilinear mask patterns are gradually adopted in industry to expand process windows, yet mainstream models are inefficient at handling such curvilinear geometries. Additionally, partial coherent illumination (PCI), a typical working condition in EUV lithography, requires numerous independent simulations across multiple source points, further exacerbating the computational burden.

Under these technical constraints, full-chip EUV MO that simultaneously accounts for high-precision thick mask effects, curvilinear patterns, and PCI has long suffered from low computational efficiency, excessive memory consumption, and poor engineering feasibility, becoming a critical bottleneck for the development of advanced computational lithography.

In a new paper published in Light: Advanced Manufacturing, a team led by Prof. Shiyuan Liu from Huazhong University of Science and Technology proposes an integrated full-chip EUV curvilinear MO framework that merges deep-learning-enabled forward modeling and gradient-based inverse optimization, providing a systematic solution to the long-standing computational and memory challenges.

The team constructs a tunable U-Net surrogate model using high-quality training data generated from an EUV mask model based on the modified Born series. This model characterizes three-dimensional thick mask effects via amplitude and phase perturbations, and eliminates redundant interference arising from incident angles through standardized preprocessing including background removal and phase unwrapping, thereby greatly reducing model complexity and enabling fast and accurate prediction of mask near fields across various source points.

The study introduces a slice-based approximated gradient calculation scheme using the adjoint method. It reforms conventional full 3D field folding computation into a spatial unfolding scheme, effectively suppressing severe gradient fluctuations along the depth direction. This approach only requires a single slice of the mask near field for gradient computation, avoiding storing the entire 3D field data, drastically reducing memory usage, and supporting large-scale parallel computing and full-chip-scale optimization.

The team validates the framework using a typical BigMaC pattern with a wafer critical dimension of 19.41 nm. The optimization proceeds in three stages, with source points gradually increasing, and the cost function converges steadily. The optimized mask patterns effectively compensate for thick mask effects, and the wafer imaging contours are greatly improved and highly consistent with the target contours. Critical dimension measurements show that the relative errors between the surrogate model and the reference model are all below 3.5%, fully verifying the high precision and reliability of the proposed framework.

This framework breaks through the bottlenecks of conventional methods and makes full-chip EUV curvilinear mask optimization computationally feasible within a practical time. It is expected to provide key algorithmic support for next-generation advanced IC manufacturing and can be further extended to high-NA EUV lithography, source-mask co-optimization, and other cutting-edge directions.

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