

Photonic spiking reinforcement learning for intelligent routing

SHANNON, CLARE, IRELAND, May 22, 2026 /EINPresswire.com/ -- Photonic spiking reinforcement learning for intelligent routing

Announcing a new publication from Opto-Electronic Sciences; DOI 10.29026/oes.2026.260005.

Intelligent routing is critical for data centers and 6G but limited by high power and latency. A photonic spiking reinforcement learning architecture with PPO was proposed for intelligent routing. Evaluated on fat-tree SDN, it outperforms Dijkstra in throughput, latency, packet loss and load balance. A hardware-software framework using MZI and DFB-SA chips achieves consistent accuracy. This low-latency, high-efficiency paradigm has broad prospects in data centers, satellite networks and 6G.

Driven by the rapid development of cloud computing, big data, artificial intelligence, and the Internet of Things, global data traffic has grown explosively, imposing unprecedented stringent requirements on the real-time performance, throughput, and energy efficiency of communication networks. In contrast to traditional routing algorithms, which rely on static link weights, lack dynamic awareness, and suffer from slow convergence, intelligent routing based on deep reinforcement learning can perceive network states in real time. It features multi-objective collaborative optimization and adaptive decision-making, showing broad application prospects in data centers, computing power networks, and future 6G scenarios.

However, neural networks implemented on conventional electronic platforms face bottlenecks such as high power consumption and large decision latency, which can hardly meet the demands of edge real-time control and large-scale high-speed, highly dynamic networks.

Photonic computing has become a key technical route to break through the bottlenecks of electronic computing due to its ultra-high speed, large bandwidth, low power consumption, and parallelism. Furthermore, spiking neural networks (SNNs) inspired by biological brain mechanisms further improve energy efficiency through event-driven computation. How to combine photonic spiking neural computing with reinforcement learning to build an intelligent routing system with ultra-low latency and ultra-high energy efficiency has become a critical scientific issue at the intersection of optical communications and artificial intelligence.

The authors of this article propose a novel software-defined networks (SDN) intelligent routing architecture based on photonic spiking reinforcement learning, providing a novel technical path

for next-generation intelligent networks.

This approach aims to construct a low-latency, high-efficiency, and adaptive intelligent routing system. The research group proposes and implements a photonic spiking reinforcement learning-based intelligent routing system for SDN, which deeply integrates SNN, proximal policy optimization (PPO), and photonic computing chips, with systematic verification carried out on a fat-tree data center topology. A three-tier architecture including data plane, control plane, and intelligent decision-making plane is designed. By employing photonic computing hardware to perform core routing decision computations, the system achieves real-time perception of network states and dynamic optimization of routing strategies, successfully overcoming the poor adaptability of traditional routing algorithms as well as the high latency and power consumption of electronic solutions.

With the MZI-based photonic synapse chip and DFB-SA-based photonic spiking neuron chip, they built a hardware-software collaborative inference platform, where the spiking Actor network is deployed on photonic hardware to maximize the speed and energy efficiency advantages of photonic computing while ensuring training stability. Experimental results on 640 state-action pairs show that the inference accuracy of the hardware-software collaborative framework is fully consistent with that of the pure software algorithm. Under various traffic loads, the proposed photonic spiking PPO routing significantly outperforms the classical Dijkstra algorithm in four key metrics: throughput, packet loss rate, average latency, and load balance, especially under high-load conditions. The system also exhibits strong robustness and fast re-convergence capability under topology changes such as link failures.

This achievement represents the first full integration of photonic spiking reinforcement learning and SDN intelligent routing, establishing a novel paradigm for routing optimization with ultra-low latency and ultra-high energy efficiency. It is expected to be applied in large-scale data centers, computing power networks, satellite Internet, and future 6G networks, providing key technical support for space-air-ground integrated real-time network optimization and advancing interdisciplinary research at the interface of photonic intelligence and communication networks.

Keywords: photonic spiking neural network, spiking reinforcement learning, intelligent routing, SDN

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Weitao Pan is an Associate Professor and Master's Supervisor, Xidian University. He has long been engaged in research on FPGA implementation and chip design for high-performance network switching architectures. He has extensive experience in satellite-borne routing and switching systems, Time-Triggered Ethernet (TTE) deterministic networks, RDMA smart network cards, and hardware architecture design and engineering implementation of AI inference accelerators. He has led or participated in a number of national major research projects and successfully taped-out multiple chips including the HINOC series (4 generations), TITAN network processor (UMC 28 nm, 16-core 1.2 GHz, quad 40 Gbps line-rate processing), and secure smart network cards. More than ten sets of core IP cores for satellite-borne routers, switches and end systems developed by him have been in-orbit operation, deployed on low-Earth orbit satellites for satellite Internet, Tianzhou-5 cargo spacecraft of China Space Station, new-generation manned spacecraft and other aerospace models. In 2023, he received First Prize of Shaanxi Science and Technology Progress Award and First Prize of Excellent Scientific Research Achievements of Shaanxi Universities. His research results have been published in journals and conferences including IEEE TC, IEEE TVLSI, IEEE TNNLS, IEEE TCAS-II, ICCAD, DAC, with more than 100 authorized invention patents. His current research focuses on domain-specific accelerator architecture design and FPGA engineering implementation for satellite-borne intelligent computing.

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ISSN 2097-0382

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Xiang SY, Chen YH, Zheng L et al. Photonic spiking reinforcement learning for intelligent routing. Opto-Electron Sci 5, 260005 (2026). DOI: 10.29026/oes.2026.260005

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