

Quantum Elements and USC Advance Noisy Quantum Circuit Simulation with New Quantum Monte Carlo Algorithm

In peer-reviewed paper, researchers describe how algorithm supports digital twins for quantum error correction and fault-tolerant system design



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[Quantum Elements](#) and USC today announced the publication of a new Quantum Monte Carlo algorithm in Physical Review Letters, providing a more efficient way to simulate noisy quantum circuits on classical computers and supporting the company's development of digital twins for quantum error correction.

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*Izhar Medalsy, co-founder
and CEO of Quantum
Elements*

The [peer-reviewed paper](#), Real-Time Sign-Problem-Suppressed Quantum Monte Carlo Algorithm for Noisy Quantum Circuit Simulations, was co-authored by Dr. Tong Shen, quantum research scientist at Quantum Elements and a postdoctoral researcher at USC, and USC Professor Daniel A. Lidar, co-founder and Chief Scientific Officer of Quantum Elements.

While quantum processors are becoming increasingly sophisticated, they are still affected by environmental

noise, crosstalk between qubits, and control imperfections. These effects are obstacles to developing fault-tolerant quantum computers. To study this behavior, researchers often simulate quantum systems on classical computers. One way to do this is direct density-matrix simulation, which tracks a noisy quantum system, including both its quantum state and its interaction with the environment. However, the amount of information required to represent the system becomes prohibitive as qubit counts grow.

The Quantum Monte Carlo algorithm presented by Quantum Elements in PRL compresses the simulation, which allows researchers to model noisy quantum-circuit behavior with lower computational resources while preserving the dynamics needed to study quantum error

correction, correlated noise, and decoder performance.

“Fault tolerance will require a much tighter feedback loop between hardware, control, simulation and decoding,” said Izhar Medalsy, co-founder and CEO of Quantum Elements. “This gives us a rigorous algorithmic foundation for building digital twins that capture the noise behavior hardware teams need.”

The practical application of this method was demonstrated in an [AWS collaboration](#) with Quantum Elements, USC, and Harvard, where researchers used a Quantum Monte Carlo-accelerated digital twin to simulate a 97-physical-qubit, distance-7 surface-code syndrome-extraction round on classical high-performance computing infrastructure. AWS reported that a brute force, full open-system simulation of the same system would require tracking 497 density-matrix entries, while the QMC-based method ran in about an hour on a single compute node.” AWS helped translate the peer-reviewed methodology into an AWS architecture, leveraging AWS ParallelCluster to deploy the Quantum Elements digital twin as a containerized workload. The solution scales horizontally across multiple instances, making it well suited for a large number of qubits.

“This is peer-reviewed evidence of what we demonstrated earlier this year in collaboration with Quantum Elements, and we look forward to leveraging AWS’ classical and quantum compute resources in conjunction with their digital twin technology to accelerate the path towards fault tolerance via quantum error correction,” said Michael Brett, Worldwide Go-To-Market Strategy Lead for Quantum Technologies at AWS.

The result comes as quantum hardware teams increasingly focus on quantum error correction as the route to useful, fault-tolerant systems. As devices scale, the engineering challenge lies in understanding how real noise affects logical performance and how software, controls, and decoding can compensate for it.

About Quantum Elements

Founded in 2023 in Los Angeles, Quantum Elements develops software for modeling, simulating, and optimizing quantum computing systems. The company is building hardware-calibrated quantum digital twins designed to help quantum hardware teams understand noise, test error-correction strategies, evaluate decoder performance, and shorten the path from experimental hardware to fault-tolerant system design.

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