

Agnisys to Showcase Agentic AI, Network-on-Chip, and DFT Automation Breakthroughs at DAC 2026

Agnisys will showcase IDS-AI™, IDS-NoC™, and Advance DFT Automation at DAC 2026 to accelerate chip design, improve quality, and speed SoC development.

GARLAND, TX, UNITED STATES, July 22, 2026 /EINPresswire.com/ -- Agnisys, Inc. is the leading provider of intelligent specification automation solutions for semiconductor design and verification, today announced it will showcase its latest innovations including [IDS-AI™](#), [IDS-NoC™](#), and advanced Design-for-Test (DFT) automation at the 63rd Design Automation Conference (DAC 2026), July 27–29 in Long Beach, CA.



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We're combining the certainty of deterministic automation with the power of AI to help semiconductor companies develop chips faster without sacrificing correctness.”

Anupam Bakshi, Founder and CEO of Agnisys, Inc.

As chip designs grow more complex with AI workloads, chiplet architectures, and safety-critical applications, Agnisys addresses these challenges with a unified automation suite spanning specification, design generation, verification, testability, validation, and documentation.

IDS-AI: From Specification to Sign-Off, Dramatically Faster
Agnisys will showcase IDS-AI, the agentic AI framework that understands semiconductor design intent and drives the entire development flow from golden specification creation to RTL sign-off. It automates specification creation, RTL generation, and verification in one connected workflow, helping teams catch defects earlier and reach sign-off

faster with correct-by-construction accuracy.

IDS-NoC: Scalable Network-on-Chip Automation

Agnisys will also showcase IDS-NoC, which automates the creation of scalable, deadlock-free Network-on-Chip fabrics for AI accelerators, automotive platforms, and multi-core SoCs. Teams generate complete, open SystemVerilog RTL fabrics instead of hand-building routers and interfaces, accelerating integration and time-to-market.

Advanced DFT Automation: Testability Built Into the Design Flow

Agnisys will present new DFT automation research at DAC 2026, introducing Design-Aware Test Points (DATP) built into the SystemRDL-to-RTL flow. Early adopters have seen up to 4× improvement in Test Coverage Per Flip-Flop (TCPF) and 50% fewer top-level ATPG patterns. This talk will be presented by Veerabhadra Rao Vasa and Rajesh Gottumukkala of Google and Freddy Nunez of Agnisys on July 28, 2026, in Seaside Room 7.

Our AI-driven solutions deliver predictable, correct-by-construction results while significantly reducing token costs. Whether you're a startup building the next breakthrough AI chip or an established semiconductor company tackling increasingly complex SoCs, or overuse of AI tokens, we'd love to discuss how deterministic AI can accelerate your design and verification flow.

Visit Agnisys at Booth #1557

Engineering leaders, architects, verification engineers, and SoC designers are invited to Booth #1557 during DAC 2026 for live demonstrations and to meet with Agnisys experts. To schedule a meeting or learn more, contact marcom@agnisys.com or visit agnisys.com/agnisys-at-dac-2026.

Upcoming Webinar

Following DAC 2026, Agnisys will host an exclusive technical webinar, "[AI-Based CSR Signoff Verification for Faster SoC Development](#)," on August 20, 2026.

The webinar will demonstrate how AI-driven automation enables engineering teams to verify CSR implementations faster, improve verification quality, eliminate manual signoff processes, and accelerate SoC development from specification to silicon. Additional registration details will be available on the Agnisys website.

About Agnisys

Agnisys is the leading provider of intelligent specification automation solutions for semiconductor development. With two decades of expertise, its IDesignSpec™ Suite takes teams from specification to sign-off, and solutions built on it, including IDS-AI™ and IDS-NoC™, combine

AGNISYS
SYSTEM DEVELOPMENT WITH CERTAINTY

THE CHIPS TO SYSTEMS CONFERENCE
SHAPING THE NEXT GENERATION OF ELECTRONICS

Automating DFT Intelligence:

Addressing TCPF Hotspots at Source Through Design-Aware Test Points in Systemrdl-to-RTL Generators

Presenters:
Veerabhadra Rao Vasa - Google
Rajesh Gottumukkala - Google
Freddy Nunez - Agnisys

Date & Time: July 28, 2026 / 11:15 - 11:30 AM PDT
Venue: Seaside RM 7

correct-by-construction automation with agentic AI to transform executable specifications into automated design, verification, DFT, and documentation deliverables. Agnisys products improve productivity, quality, and time-to-market for SoC, ASIC, FPGA, IP, and AI-driven chip development worldwide.

Tom Anderson

Agnisys, Inc.

marcom@agnisys.com

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