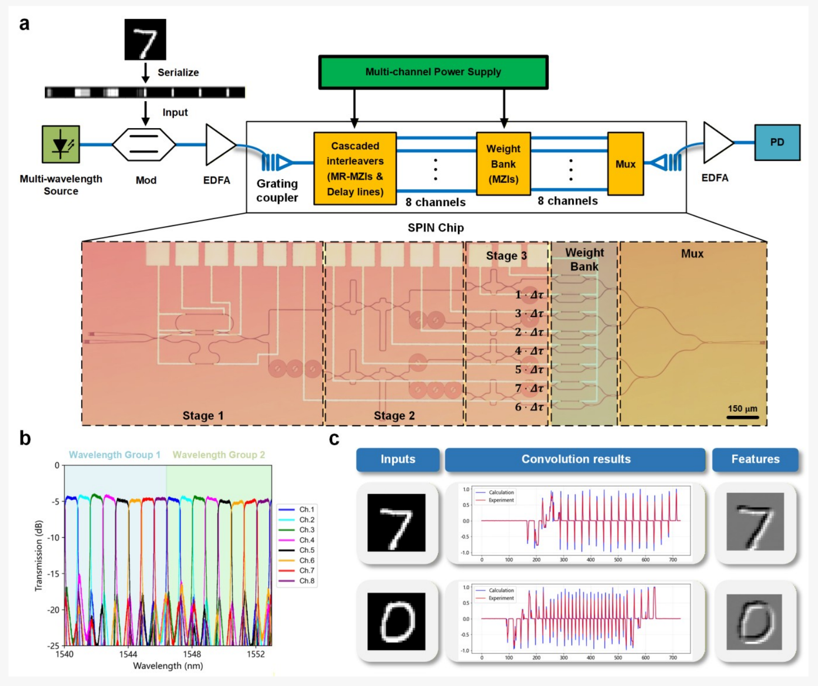
High-Density Integrated Photonic Convolution: A Scalable Spatiotemporal Interleaving Network

A compact silicon photonic architecture shifts convolution scaling from spatial replication to wavelength-domain interleaving

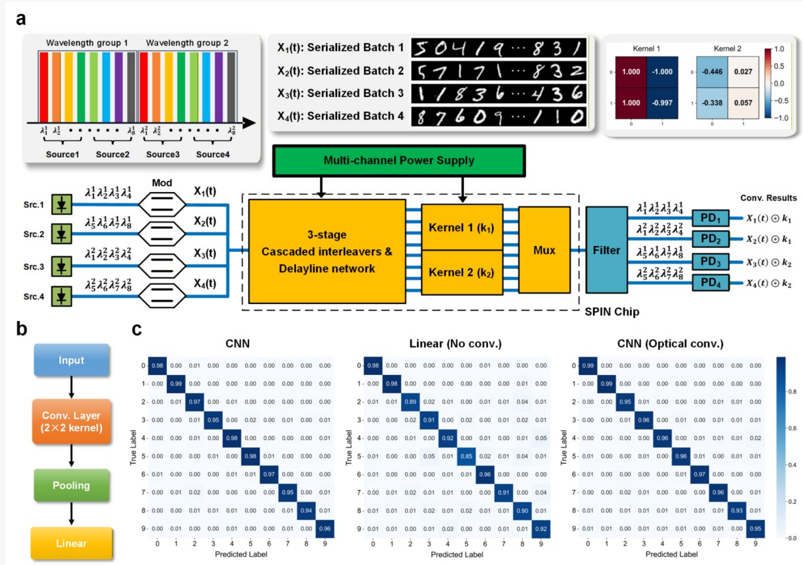


The fabricated SPIN chip executes optical convolution on handwritten-digit inputs; measured temporal waveforms agree with digital ground truth and reconstruct clear feature maps.

CHINA, August 3, 2026 /EINPresswire.com/ -- Researchers at Shanghai Jiao Tong University present SPIN, a spatiotemporal photonic interleaving network for scalable photonic convolution. By recursively sharing optical delay lines across wavelength channels, SPIN reduces waveguide-length scaling from $O(K^2)$ to $O(K \log\square K)$ and active control elements to $O(K)$. Experiments on MNIST digits show optical–digital correlations above 0.98, while analysis projects 29.7 TOPS from one populated spectral core. The design also supports programmable kernel geometry and wavelength-multiplexed task parallelism.

Modern artificial intelligence and image-processing workloads require hardware that can execute convolution with high throughput, compact footprint, and practical energy consumption. Conventional electronic accelerators continue to improve, but large-scale convolution and matrix operations are increasingly constrained by data movement, interconnect overhead, and chip-area scaling rather than by arithmetic units alone.

Integrated photonics offers a complementary route because light can carry many signals in parallel through wavelength, time, and space. Photonic processors are particularly attractive for linear operations such as convolution and matrix–vector multiplication, which are central to machine vision and neural networks. However, existing photonic architectures face their own trade-offs. Mach-Zehnder interferometer meshes can be programmable but scale poorly in footprint and control complexity. Microring resonators are compact but sensitive to temperature and fabrication variations. Diffractive or metasurface approaches can be dense, yet are often difficult to reconfigure once fabricated.



Multiple wavelength groups share the same on-chip photonic core, enabling parallel convolution tasks without replicating the complete physical computing network.

The research group of Professor Yikai Su from Shanghai Jiao Tong University addresses this density–programmability challenge with a spatiotemporal photonic interleaving network, or SPIN. Instead of increasing throughput mainly by copying more spatial optical paths, SPIN redistributes the scaling burden into the wavelength dimension. The result is a compact and programmable photonic convolution framework for high-density optical computing. The study was published in the journal Opto-Electronic Science on July 23, 2026.

SPIN is built around a recursive tree of cascaded optical interleavers. A serialized input waveform is broadcast onto multiple wavelength carriers, and each wavelength is routed through a designed sequence of shared delay segments. These delays create the time-aligned sliding window needed for convolution. Kernel weights are then applied optically, the weighted signals are incoherently summed, and the signed convolution result is recovered electronically after baseline subtraction.

This topology changes how convolution scales on chip. In a conventional independent-delay design, larger kernels require many separate delay paths, causing the total waveguide length to grow quadratically with the number of operands. SPIN places longer delay segments upstream in the interleaver tree, where they are reused by multiple downstream wavelength channels. The authors show that this reduces waveguide-length complexity to $O(K \log_2 K)$, while the number of actively controlled weighting elements grows only as $O(K)$.

The team fabricated a proof-of-concept SPIN chip on a commercial 220 nm silicon-on-insulator platform. The prototype uses a three-stage cascaded interleaver network for eight wavelength channels. In experiments at 49 Gbaud, the chip performed representative 2 × 2 convolution operations on MNIST handwritten digits. The measured optical waveforms agreed closely with digital ground truth, with correlation coefficients above 0.98, and the reconstructed feature maps clearly highlighted digit contours.

Beyond single-task convolution, the authors demonstrated wavelength-domain scalability. Sixteen optical carriers were divided into wavelength groups so that multiple image batches and convolution tasks could share the same physical SPIN core. The paper also shows structural reconfigurability by implementing a 2 × 4 convolution kernel on natural images from the USC-SIPI database. This ability to trade wavelength resources among kernel size, geometry, patch parallelism, and task parallelism is central to the architecture.

The projected performance is also scalable. When available spectrum is fully exploited, the authors estimate that a single SPIN core could approach 29.7 TOPS. While practical systems will still require co-design of modulators, photodetectors, frequency-comb sources, calibration, and electronic interfaces, SPIN provides a clear route toward compact, high-throughput, and reconfigurable photonic accelerators for optical convolution.

Reference
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This research was conducted by the team led by Professor Yikai Su from the State Key Laboratory of Photonics and Communications at the School of Information Science and Electronic Engineering | Integrated Circuits, Shanghai Jiao Tong University. Prof. Su's Optical Transmission and Integrated Photonics Laboratory (OTIP) mainly studies high-speed optical communication systems and various integrated devices, focusing on silicon-based and heterogeneously-integrated photonic chips for photonic transmission and switching.

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